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40	BOM

# IH11D-MHS

## VER 7.0

### CPU:

**Intel Skylake S 42 in LGA1151 Package 80W**

### System Chipset:

**H110**

### Main Memory:

**Dual Channel/DDR-III\*2(Max 16GB) 1066/1333/1600**

### Onboard Device:

**Super I/O:IT8613E**

**LAN:Realtek 8111H**

**HD Codec:ALC887**

### Power solution:

**CPU Voltage Regulators:3phase by RT3606**

**GT Voltage Regulators:1phase by RT3606**

**DDR Voltage Regulators:1Phase by UP1514**

### Expansion Slots:

**PCI EXPRESS 16X SLOT \*1**

**PCI EXPRESS 1X SLOT \*1**

### REAR IO:

**PS/2 PORT**

**HDMI Port**

**VGA Port**

**USB3.0 PORT**

**Gb RJ-45 +2 layer USB2.0 Port**

**Audio Jackets (3 PORT)**

### Front I/O:

**SATA3 \*4**

**USB 2.0 Header \* 2**

**USB 3.0 Header \* 1**

**CPU FAN \*1**


**System FAN \*1**

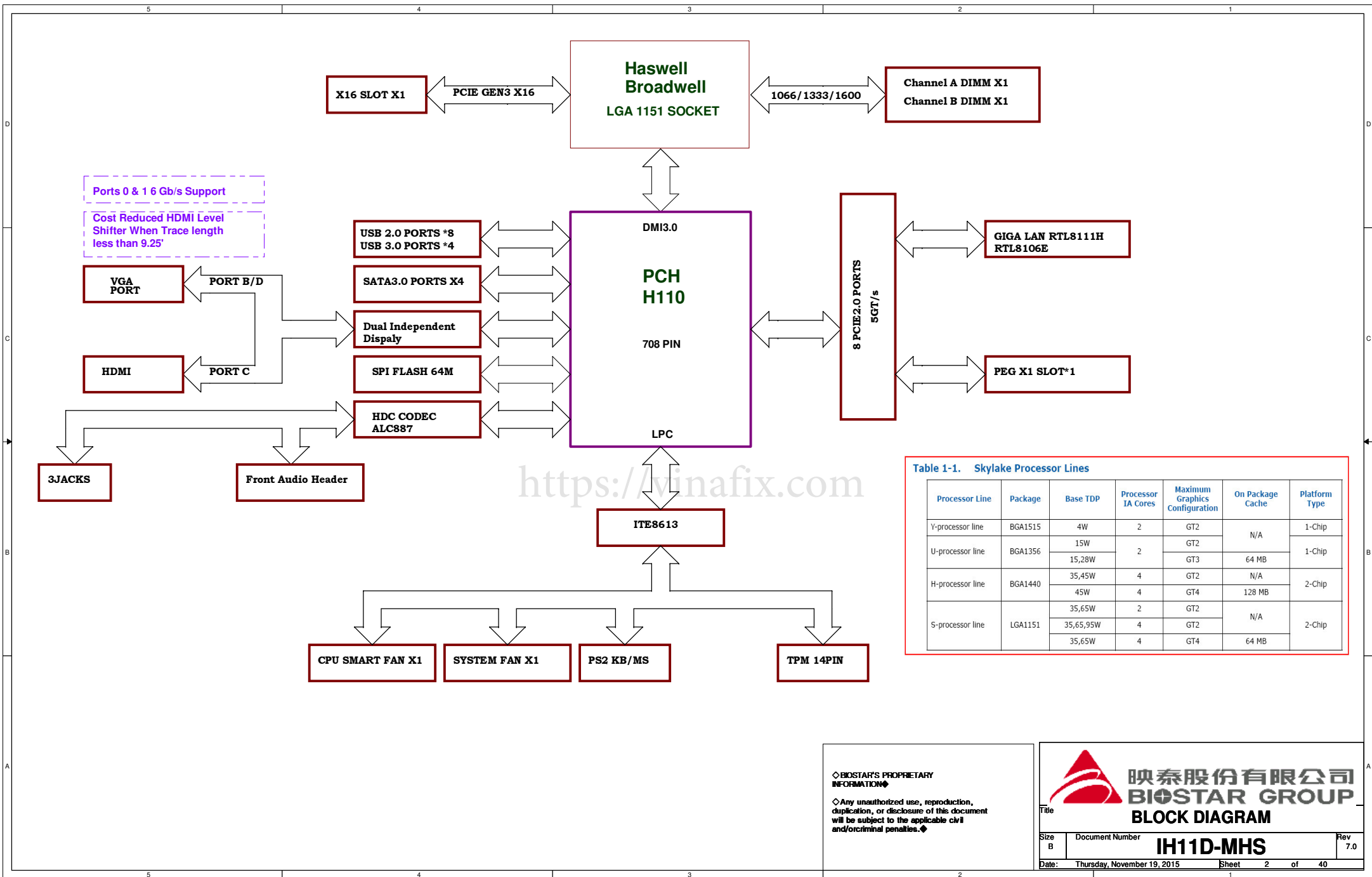
**Front Audio Header**

**TPM14 Header \* 1**


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**HW ELI**

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			<b>映泰股份有限公司</b> <b>BIOSTAR GROUP</b>		
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2.VER0.60:REMOVE Hi-Fi FUNCTION(PAGE23/28/29)

3.VER0.60:CHANGE CPU POWER CONN TO 2\*2(PAGE39)

4.VER0.60:NEW ADD COLAY FOR V\_SA\_IO(PAGE38)

5.VER0.6:COST DOWN(POWER\_JUSB1 COLAY POWER\_JUSB2) (PAGE26)

6.VER0.6:COST DOWN(REMOVE CT6) (PAGE26)

7.VER0.6:COST DOWN(MODIFY F6/GF3 SIZE) (PAGE21/34)

8.VER0.6:COST DOWN(MODIFY MC36 SIZE) (PAGE11)

9.VER0.6:COST DOWN(MCT2/3/CT11 CHANGE TO 560UF) (PAGE31/32)

10.VER0.6:COST DOWN(MC38 /NI) (PAGE11)

11.VER0.6:COST DOWN(YC23 /NI) (PAGE18)

12.VER0.6:COST DOWN(YC16/17/21 /NI) (PAGE18)

13.VER0.6:COST DOWN(LC18/MC5/6 CHANGE TO 10UF 0603 SIZE) (PAGE11/27)

14.VER0.6:COST DOWN(PC155 CHANGE TO 10UF 0603 SIZE) (PAGE39)

15.VER0.6:COST DOWN(C165/MC9 CHANGE TO 1UF 0805 SIZE) (PAGE31/38)

16.VER0.6:COST DOWN(YC11/26 /NI) (PAGE18)

17.VER0.6:COST DOWN(CHANGE TO RN 8P4R) (PAGE17)

18.VER0.6:ATXPG MODIFY(PAGE23/36)

19.VER0.6:COST DOWN(PAGE33)

20.VER0.6:COST DOWN(2N7002 CHANGE TO 2N3904) (PAGE30/33/39)

21.VER0.6:COST DOWN(SHORT 0402) (PAGE8/11/12/16/19/23/33/39)

22.VER0.6:COST DOWN(SHORT 0805) (PAGE18/37/39/40)

23.VER0.6:COST DOWN(BEAD COLAY) (PAGE29)

24.VER0.6:COST DOWN(CPU PWM CHANHE TO RT3606) (PAGE39/40/41)

25.VER0.6:COST DOWN(POWER\_JUSB4/POWER\_JUSB5 COLAY) (PAGE25/34)

26.VER0.6:MIC MODIFY BY KEVIN(PAGE28)

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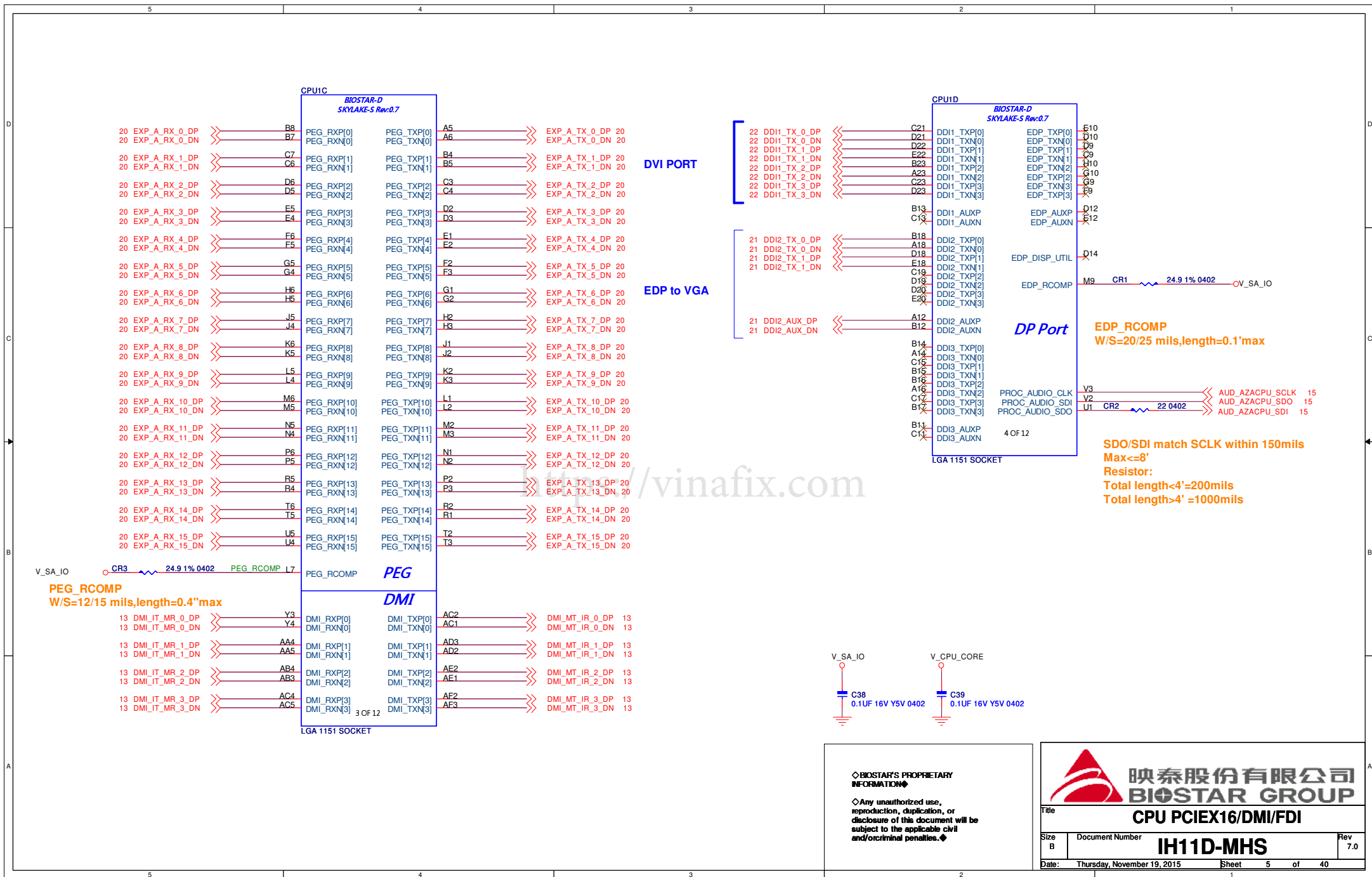


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Title  
**CHANGELIST**

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11 M\_DATA\_A[0..63] <<> M\_DATA\_A[0..63]

M\_DATA\_A0 AE38  
M\_DATA\_A1 AE37  
M\_DATA\_A2 AG38  
M\_DATA\_A3 AG37  
M\_DATA\_A4 AE39  
M\_DATA\_A5 AE40  
M\_DATA\_A6 AG39  
M\_DATA\_A7 AG40  
M\_DATA\_A8 AJ38  
M\_DATA\_A9 AJ37  
M\_DATA\_A10 AL38  
M\_DATA\_A11 AL37  
M\_DATA\_A12 AJ40  
M\_DATA\_A13 AJ39  
M\_DATA\_A14 AL39  
M\_DATA\_A15 AL40  
M\_DATA\_A16 AN38  
M\_DATA\_A17 AN40  
M\_DATA\_A18 AR38  
M\_DATA\_A19 AR37  
M\_DATA\_A20 AN39  
M\_DATA\_A21 AN37  
M\_DATA\_A22 AR39  
M\_DATA\_A23 AR40  
M\_DATA\_A24 AW37  
M\_DATA\_A25 AU38  
M\_DATA\_A26 AV38  
M\_DATA\_A27 AW39  
M\_DATA\_A28 AU37  
M\_DATA\_A29 AV37  
M\_DATA\_A30 AT35  
M\_DATA\_A31 AU35  
M\_DATA\_A32 AY8  
M\_DATA\_A33 AW8  
M\_DATA\_A34 AV6  
M\_DATA\_A35 AU8  
M\_DATA\_A36 AU8  
M\_DATA\_A37 AV8  
M\_DATA\_A38 AW8  
M\_DATA\_A39 AY6  
M\_DATA\_A40 AY4  
M\_DATA\_A41 AV4  
M\_DATA\_A42 AT1  
M\_DATA\_A43 AT2  
M\_DATA\_A44 AV3  
M\_DATA\_A45 AW4  
M\_DATA\_A46 AT4  
M\_DATA\_A47 AT3  
M\_DATA\_A48 AP2  
M\_DATA\_A49 AM4  
M\_DATA\_A50 AP3  
M\_DATA\_A51 AM3  
M\_DATA\_A52 AP4  
M\_DATA\_A53 AM2  
M\_DATA\_A54 AP1  
M\_DATA\_A55 AM1  
M\_DATA\_A56 AK3  
M\_DATA\_A57 AH1  
M\_DATA\_A58 AK4  
M\_DATA\_A59 AH2  
M\_DATA\_A60 AH4  
M\_DATA\_A61 AK2  
M\_DATA\_A62 AH3  
M\_DATA\_A63 AK1

CPU1A

BIOSTAR-D  
SKYLAKE-S Rev0.7

DDR CHANNEL A

DDR0\_DQ[0]  
DDR0\_DQ[1]  
DDR0\_DQ[2]  
DDR0\_DQ[3]  
DDR0\_DQ[4]  
DDR0\_DQ[5]  
DDR0\_DQ[6]  
DDR0\_DQ[7]  
DDR0\_DQ[8]  
DDR0\_DQ[9]  
DDR0\_DQ[10]  
DDR0\_DQ[11]  
DDR0\_DQ[12]  
DDR0\_DQ[13]  
DDR0\_DQ[14]  
DDR0\_DQ[15]  
DDR0\_DQ[16]/DDR0\_DQ[32]  
DDR0\_DQ[17]/DDR0\_DQ[33]  
DDR0\_DQ[18]/DDR0\_DQ[34]  
DDR0\_DQ[19]/DDR0\_DQ[35]  
DDR0\_DQ[20]/DDR0\_DQ[36]  
DDR0\_DQ[21]/DDR0\_DQ[37]  
DDR0\_DQ[22]/DDR0\_DQ[38]  
DDR0\_DQ[23]/DDR0\_DQ[39]  
DDR0\_DQ[24]/DDR0\_DQ[40]  
DDR0\_DQ[25]/DDR0\_DQ[41]  
DDR0\_DQ[26]/DDR0\_DQ[42]  
DDR0\_DQ[27]/DDR0\_DQ[43]  
DDR0\_DQ[28]/DDR0\_DQ[44]  
DDR0\_DQ[29]/DDR0\_DQ[45]  
DDR0\_DQ[30]/DDR0\_DQ[46]  
DDR0\_DQ[31]/DDR0\_DQ[47]  
DDR0\_DQ[32]/DDR1\_DQ[0]  
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DDR0\_DQ[59]/DDR1\_DQ[43]  
DDR0\_DQ[60]/DDR1\_DQ[44]  
DDR0\_DQ[61]/DDR1\_DQ[45]  
DDR0\_DQ[62]/DDR1\_DQ[46]  
DDR0\_DQ[63]/DDR1\_DQ[47]  
DDR0\_ECC[0]  
DDR0\_ECC[1]  
DDR0\_ECC[2]  
DDR0\_ECC[3]  
DDR0\_ECC[4]  
DDR0\_ECC[5]  
DDR0\_ECC[6]  
DDR0\_ECC[7]

AL39  
AT32  
AW32  
AV32  
AU32  
AV32  
AW32  
AY32

LGA 1151 SOCKET

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DDR0\_CK[0]  
DDR0\_CK[1]  
DDR0\_CK[2]  
DDR0\_CK[3]  
DDR0\_CK[4]  
DDR0\_CK[5]  
DDR0\_CK[6]  
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DDR0\_CK[8]  
DDR0\_CK[9]  
DDR0\_CK[10]  
DDR0\_CK[11]  
DDR0\_CK[12]  
DDR0\_CK[13]  
DDR0\_CK[14]  
DDR0\_CK[15]  
DDR0\_CS[0]  
DDR0\_CS[1]  
DDR0\_CS[2]  
DDR0\_CS[3]  
DDR0\_ODT[0]  
DDR0\_ODT[1]  
DDR0\_ODT[2]  
DDR0\_ODT[3]

DDR0\_BA[0]/DDR0\_CAB[4]/DDR0\_BA[0]  
DDR0\_BA[1]/DDR0\_CAB[6]/DDR0\_BA[1]  
DDR0\_BA[2]/DDR0\_CAB[5]/DDR0\_BA[2]  
DDR0\_RAS#/DDR0\_CAB[3]/DDR0\_MA[16]  
DDR0\_WE#/DDR0\_CAB[2]/DDR0\_MA[14]  
DDR0\_CAS#/DDR0\_CAB[1]/DDR0\_MA[15]  
DDR0\_MA[0]/DDR0\_CAB[9]/DDR0\_MA[0]  
DDR0\_MA[1]/DDR0\_CAB[8]/DDR0\_MA[1]  
DDR0\_MA[2]/DDR0\_CAB[5]/DDR0\_MA[2]  
DDR0\_MA[3]  
DDR0\_MA[4]  
DDR0\_MA[5]/DDR0\_CAA[0]/DDR0\_MA[5]  
DDR0\_MA[6]/DDR0\_CAA[2]/DDR0\_MA[6]  
DDR0\_MA[7]/DDR0\_CAA[4]/DDR0\_MA[7]  
DDR0\_MA[8]/DDR0\_CAA[3]/DDR0\_MA[8]  
DDR0\_MA[9]/DDR0\_CAA[1]/DDR0\_MA[9]  
DDR0\_MA[10]/DDR0\_CAB[7]/DDR0\_MA[10]  
DDR0\_MA[11]/DDR0\_CAA[7]/DDR0\_MA[11]  
DDR0\_MA[12]/DDR0\_CAA[6]/DDR0\_MA[12]  
DDR0\_MA[13]/DDR0\_CAB[0]/DDR0\_MA[13]  
DDR0\_MA[14]/DDR0\_CAA[9]/DDR0\_BG[1]  
DDR0\_MA[15]/DDR0\_CAA[8]/DDR0\_ACT#


DDR0\_PAR  
DDR0\_ALERT#

DDR0\_DQSN[0]  
DDR0\_DQSN[1]  
DDR0\_DQSN[2]/DDR0\_DQSN[4]  
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DDR0\_DQSN[7]/DDR1\_DQSN[5]  
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DDR0\_DQSP[1]  
DDR0\_DQSP[2]/DDR0\_DQSP[4]  
DDR0\_DQSP[3]/DDR0\_DQSP[5]  
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DDR0\_DQSP[5]/DDR1\_DQSP[1]  
DDR0\_DQSP[6]/DDR1\_DQSP[4]  
DDR0\_DQSP[7]/DDR1\_DQSP[5]  
DDR0\_DQSP[8]  
DDR0\_DQSN[8]

AW18 >>> CK\_M\_CH0\_0\_DP 11  
AV18 >>> CK\_M\_CH0\_0\_DN 11  
AW17 >>> CK\_M\_CH0\_1\_DP 11  
AY17 >>> CK\_M\_CH0\_1\_DN 11  
AW16 >>> M\_SCKE\_A0 11  
AV16 >>> M\_SCKE\_A1 11  
AT16 >>> M\_SCS\_A\_N0 11  
AU16 >>> M\_SCS\_A\_N1 11  
AY24 >>> M\_ODT\_A0 11  
AW24 >>> M\_ODT\_A1 11  
AV24 >>> M\_SBS\_A0 11  
AY10 >>> M\_SBS\_A1 11  
AY10 >>> M\_BG\_CH0\_0 11  
AW13 >>> M\_MAA\_A16 11  
AV14 >>> M\_MAA\_A14 11  
AY11 >>> M\_MAA\_A15 11  
AW15 >>> M\_MAA\_A0 11  
AU18 >>> M\_MAA\_A1 11  
AU17 >>> M\_MAA\_A2 11  
AV19 >>> M\_MAA\_A3 11  
AT19 >>> M\_MAA\_A4 11  
AU20 >>> M\_MAA\_A5 11  
AV20 >>> M\_MAA\_A6 11  
AU21 >>> M\_MAA\_A7 11  
AT20 >>> M\_MAA\_A8 11  
AT22 >>> M\_MAA\_A9 11  
AY14 >>> M\_MAA\_A10 11  
AU22 >>> M\_MAA\_A11 11  
AV22 >>> M\_MAA\_A12 11  
AV12 >>> M\_MAA\_A13 11  
AV23 >>> M\_BG\_CH0\_1 11  
AU24 >>> DDR\_CH0\_ACT\_N 11  
AY15 >>> DDR\_CH0\_ALERT\_N 11  
AT23 >>> DDR\_CH0\_ALERT\_N 11

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Table 51-7



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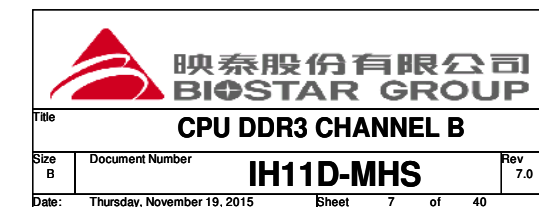
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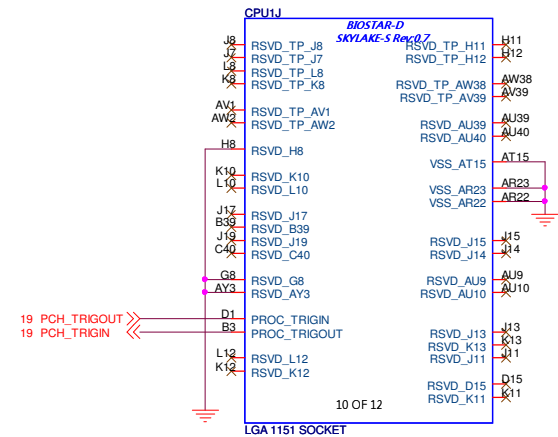
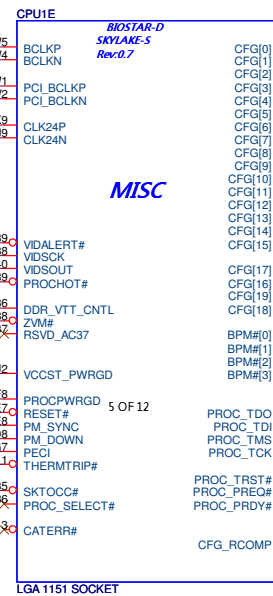
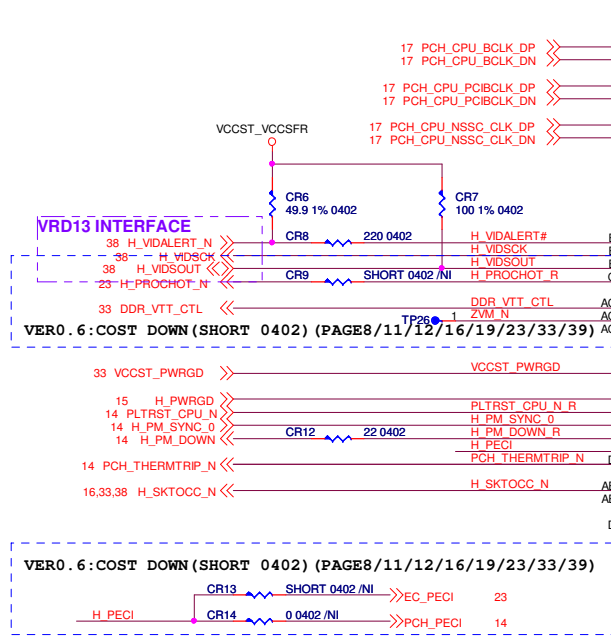
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CFG	HIGH	LOW	STRAP DESCRIPTION
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3	ENABLE	DISABLE	PHYSICAL_DEBUG_ENABLE
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVATE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI_AC_COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYN	PMSYNC ASYN MODE
14	RESERVED		
15	RESERVED		

ALL PINS HAVE INTERNAL PULL-UPS

Bifurcation	Link Width			Config. Signals		
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]
1x16	x16	N/A	N/A	1	1	1
1x16 Reversed	x16	N/A	N/A	1	1	0
2x8	x8	x8	N/A	1	0	1
2x8 Reversed	x8	x8	N/A	1	0	0
1x8+2x4	x8	x4	x4	0	0	1
1x8+2x4 Reversed	x8	x4	x4	0	0	0

**Configuration Signals:** The CFG signals have a default value of 1, if not terminated on the board, refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

**CFG[0]:** Standby reset sequence after PCU PLL lock until deasserted.  
 - 1 = (Default) Normal Operation;  
 - 0 = Standby.

**CFG[1]:** Reserved configuration lane.

**CFG[2]:** PCI Express\* Static x16 Lane Numbering Reversal.  
 - 1 = Normal operation  
 - 0 = Lane numbers reversed.

**CFG[3]:** Reserved configuration lane.

**CFG[4]:** eDP enable:  
 - 1 = Enabled.  
 - 0 = Disabled.

**CFG[5]:** PCI Express\* Bifurcation  
 - 01 = reserved  
 - 10 = 2 x8 PCI Express\*  
 - 11 = 1 x16 PCI Express\*

**CFG[6]:** PEG Training:  
 - 1 = already PEG train immediately following RESET# deassertion.  
 - 0 = PEG Wait for BIOS for training.

**CFG[7-15]:** Reserved configuration lanes.

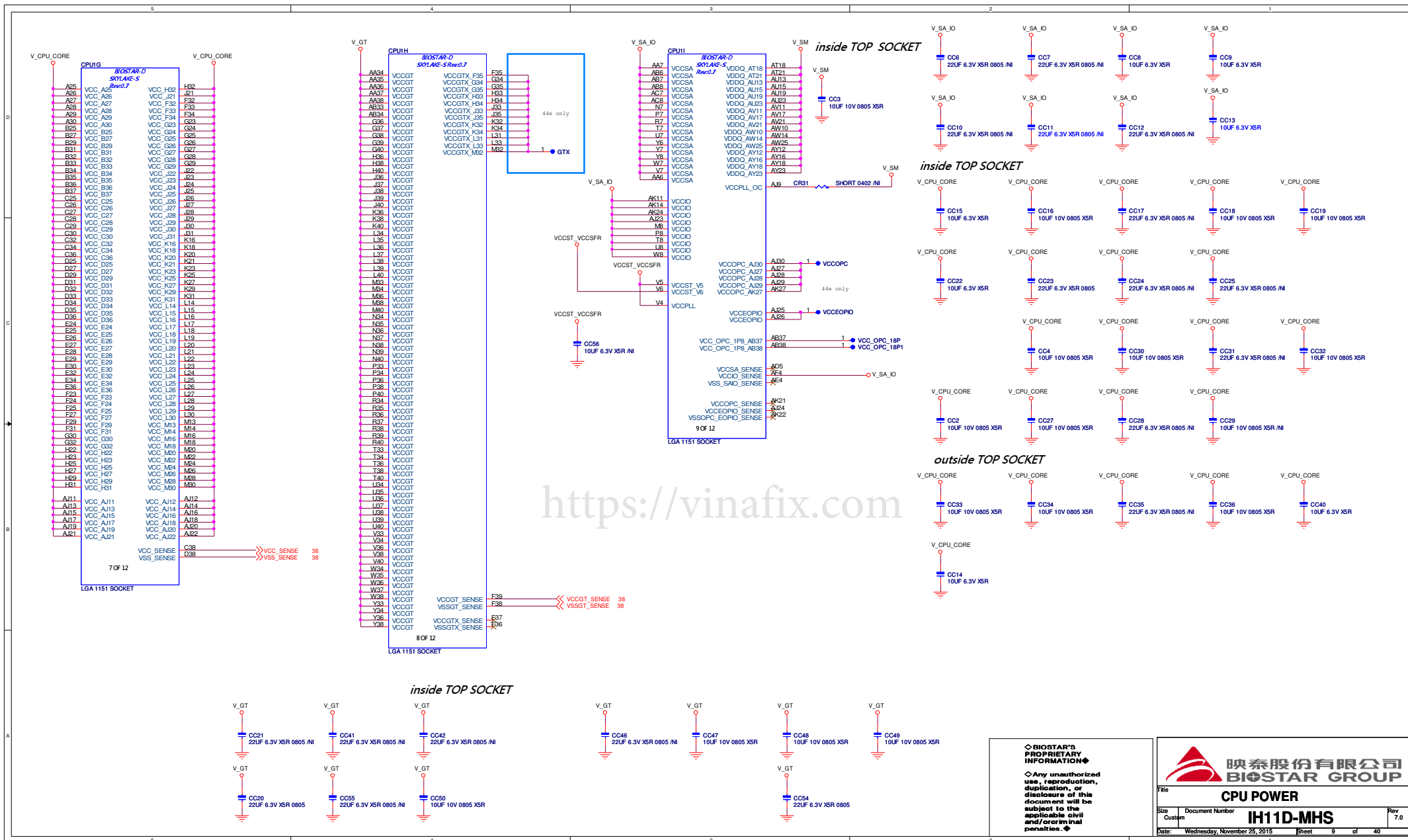
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**CPU MISC**

**CH11D-MHS**

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## CPU1K

BIOSTAR-D  
SKYLAKE-S  
Rev.0.7

A11	VSS	AK29	VSS
A13	VSS	AK30	VSS
A15	VSS	AK36	VSS
A17	VSS	AK37	VSS
A24	VSS	AK40	VSS
A7	VSS	AK5	VSS
AA3	VSS	AK6	VSS
AA33	VSS	AK7	VSS
AA8	VSS	AK8	VSS
AB39	VSS	AK9	VSS
AB5	VSS	AL1	VSS
AC3	VSS	AL11	VSS
AC33	VSS	AL14	VSS
AC34	VSS	AL2	VSS
AC35	VSS	AL21	VSS
AC6	VSS	AL24	VSS
AD1	VSS	AL27	VSS
AD33	VSS	AL3	VSS
AD36	VSS	AL30	VSS
AD37	VSS	AL36	VSS
AD38	VSS	AL4	VSS
AD39	VSS	AL5	VSS
AD4	VSS	AM11	VSS
AD40	VSS	AM14	VSS
AD6	VSS	AM17	VSS
AD7	VSS	AM19	VSS
AD8	VSS	AM24	VSS
AE3	VSS	AM27	VSS
AE33	VSS	AM30	VSS
AE36	VSS	AM31	VSS
AE5	VSS	AM32	VSS
AE8	VSS	AM33	VSS
AF1	VSS	AM34	VSS
AF33	VSS	AM35	VSS
AF36	VSS	AM36	VSS
AF37	VSS	AM37	VSS
AF40	VSS	AM38	VSS
AF5	VSS	AM39	VSS
AF8	VSS	AM40	VSS
AG1	VSS	AM5	VSS
AG2	VSS	AN1	VSS
AG3	VSS	AN10	VSS
AG33	VSS	AN11	VSS
AG36	VSS	AN14	VSS
AG4	VSS	AN16	VSS
AG5	VSS	AN19	VSS
AG8	VSS	AN22	VSS
AH33	VSS	AN23	VSS
AH36	VSS	AN24	VSS
AH37	VSS	AN27	VSS
AH38	VSS	AN30	VSS
AH39	VSS	AN36	VSS
AH40	VSS	AN4	VSS
AH5	VSS	AN5	VSS
AH8	VSS	AN6	VSS
AJ1	VSS	AN7	VSS
AJ31	VSS	AN8	VSS
AJ32	VSS	AN9	VSS
AJ33	VSS	AP11	VSS
AJ34	VSS	AP14	VSS
AJ35	VSS	AP24	VSS
AJ36	VSS	AP27	VSS
AJ4	VSS	AP30	VSS
AJ5	VSS	AP36	VSS
AJ8	VSS	AP37	VSS
AK10	VSS	AP40	VSS
AK12	VSS	B5	VSS
AK13	VSS	B6	VSS
AK15	VSS	C12	VSS
AK16	VSS	AR14	VSS
AK17	VSS	AR16	VSS
AK18	VSS	AR17	VSS
AK19	VSS	AR18	VSS
AK20	VSS	AR19	VSS
AK23	VSS	AR2	VSS
AK25	VSS	AR20	VSS
AK26	VSS	C33	VSS
AK28	VSS	C35	VSS

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LGA 1151 SOCKET

## CPU1L

BIOSTAR-D  
SKYLAKE-S Rev.0.7

AR24	VSS	C37	VSS
AR27	VSS	C5	VSS
AR3	VSS	C8	VSS
AR30	VSS	C10	VSS
AR31	VSS	D24	VSS
AR32	VSS	D26	VSS
AR33	VSS	D28	VSS
AR34	VSS	D30	VSS
AR35	VSS	D37	VSS
AR36	VSS	D39	VSS
AR4	VSS	D4	VSS
AR5	VSS	D7	VSS
AT10	VSS	E11	VSS
AT11	VSS	E13	VSS
AT12	VSS	E15	VSS
AT13	VSS	E17	VSS
AT14	VSS	E19	VSS
AT17	VSS	E21	VSS
AT24	VSS	E23	VSS
AT3	VSS	E3	VSS
AT25	VSS	E31	VSS
AT26	VSS	E33	VSS
AT27	VSS	E35	VSS
AT28	VSS	E37	VSS
AT29	VSS	E6	VSS
AT30	VSS	E9	VSS
AT31	VSS	F1	VSS
AT32	VSS	F10	VSS
AT34	VSS	F22	VSS
AT36	VSS	F26	VSS
AT37	VSS	F28	VSS
AT38	VSS	F30	VSS
AT39	VSS	F4	VSS
AT40	VSS	F40	VSS
AT5	VSS	F7	VSS
AT6	VSS	G11	VSS
AT7	VSS	G13	VSS
AT8	VSS	G15	VSS
AT9	VSS	G17	VSS
AU1	VSS	G19	VSS
AU25	VSS	G22	VSS
AU30	VSS	G3	VSS
AU34	VSS	G31	VSS
AL1	VSS	G33	VSS
AL5	VSS	G6	VSS
AN11	VSS	H1	VSS
AV2	VSS	H21	VSS
AV26	VSS	H24	VSS
AV28	VSS	H26	VSS
AV30	VSS	H28	VSS
AV34	VSS	H30	VSS
AV38	VSS	H35	VSS
AV5	VSS	H37	VSS
AV9	VSS	H39	VSS
AW3	VSS	H4	VSS
AW30	VSS	H7	VSS
AW32	VSS	H9	VSS
AW34	VSS	J10	VSS
AW7	VSS	J12	VSS
AW5	VSS	L11	VSS
AW9	VSS	L16	VSS
AY27	VSS	J18	VSS
AY30	VSS	J20	VSS
AY5	VSS	J3	VSS
AY7	VSS	J32	VSS
AP30	VSS	J34	VSS
B24	VSS	J6	VSS
AP37	VSS	K1	VSS
B28	VSS	K14	VSS
B5	VSS	K15	VSS
B6	VSS	K17	VSS
AR11	VSS	K19	VSS
AR14	VSS	K22	VSS
C16	VSS	K24	VSS
AR17	VSS	K26	VSS
C18	VSS	K28	VSS
C20	VSS	K30	VSS
AR19	VSS	K33	VSS
C22	VSS	K35	VSS
AR2	VSS	K37	VSS
C24	VSS		
AR20	VSS		
C31	VSS		
C33	VSS		
C35	VSS		

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LGA 1151 SOCKET

## CPU1F

BIOSTAR-D  
SKYLAKE-S  
Rev.0.7

K39	VSS
K4	VSS
K7	VSS
L13	VSS
L3	VSS
L32	VSS
L6	VSS
L9	VSS
M1	VSS
M10	VSS
M12	VSS
M15	VSS
M17	VSS
M19	VSS
M21	VSS
M23	VSS
M25	VSS
M27	VSS
M29	VSS
M35	VSS
M37	VSS
M39	VSS
M4	VSS
M7	VSS
N3	VSS
N33	VSS
N6	VSS
N8	VSS
P1	VSS
P35	VSS
P37	VSS
P39	VSS
P4	VSS
R3	VSS
R33	VSS
R6	VSS
R8	VSS
T1	VSS
T35	VSS
T37	VSS
T39	VSS
T4	VSS
U3	VSS
U33	VSS
U6	VSS
V1	VSS
V35	VSS
V37	VSS
V39	VSS
V8	VSS
W3	VSS
W33	VSS
W6	VSS
Y35	VSS
Y37	VSS
Y5	VSS
A4	VSS_NCTF
B38	VSS_NCTF
C2	VSS_NCTF
D40	VSS_NCTF

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LGA 1151 SOCKET

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Sheet

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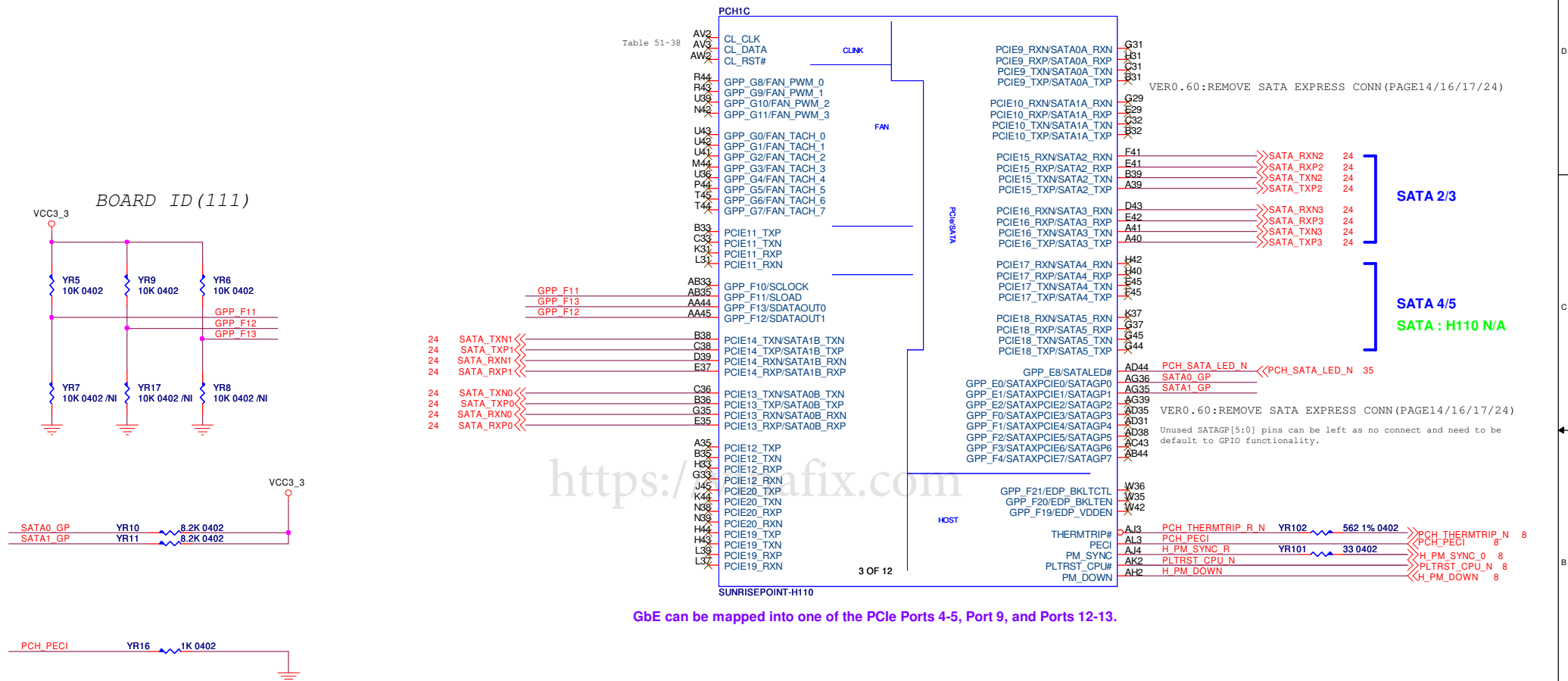




## A

A

# PCH PART: Y+Reference



GbE can be mapped into one of the PCIe Ports 4-5, Port 9, and Ports 12-13.

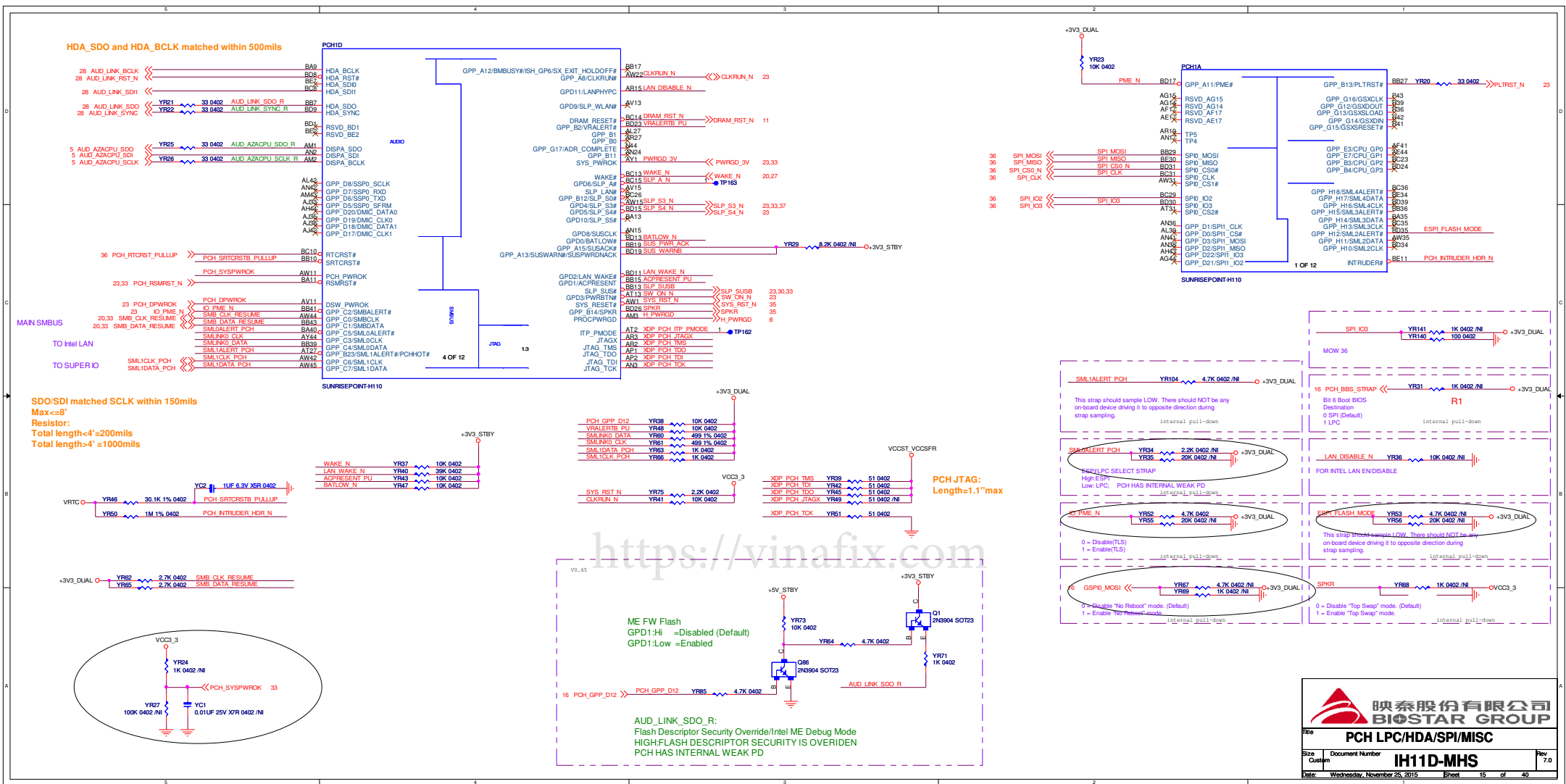
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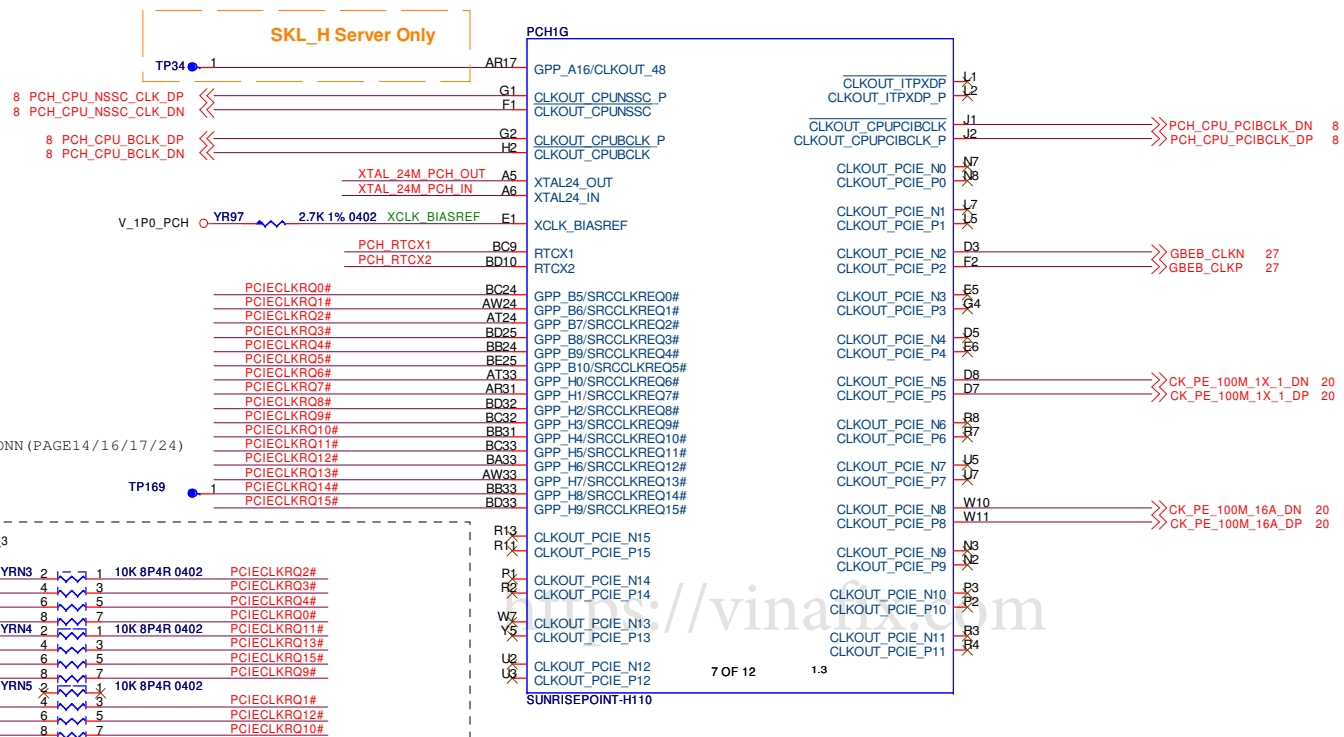
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Size	Document Number	Rev
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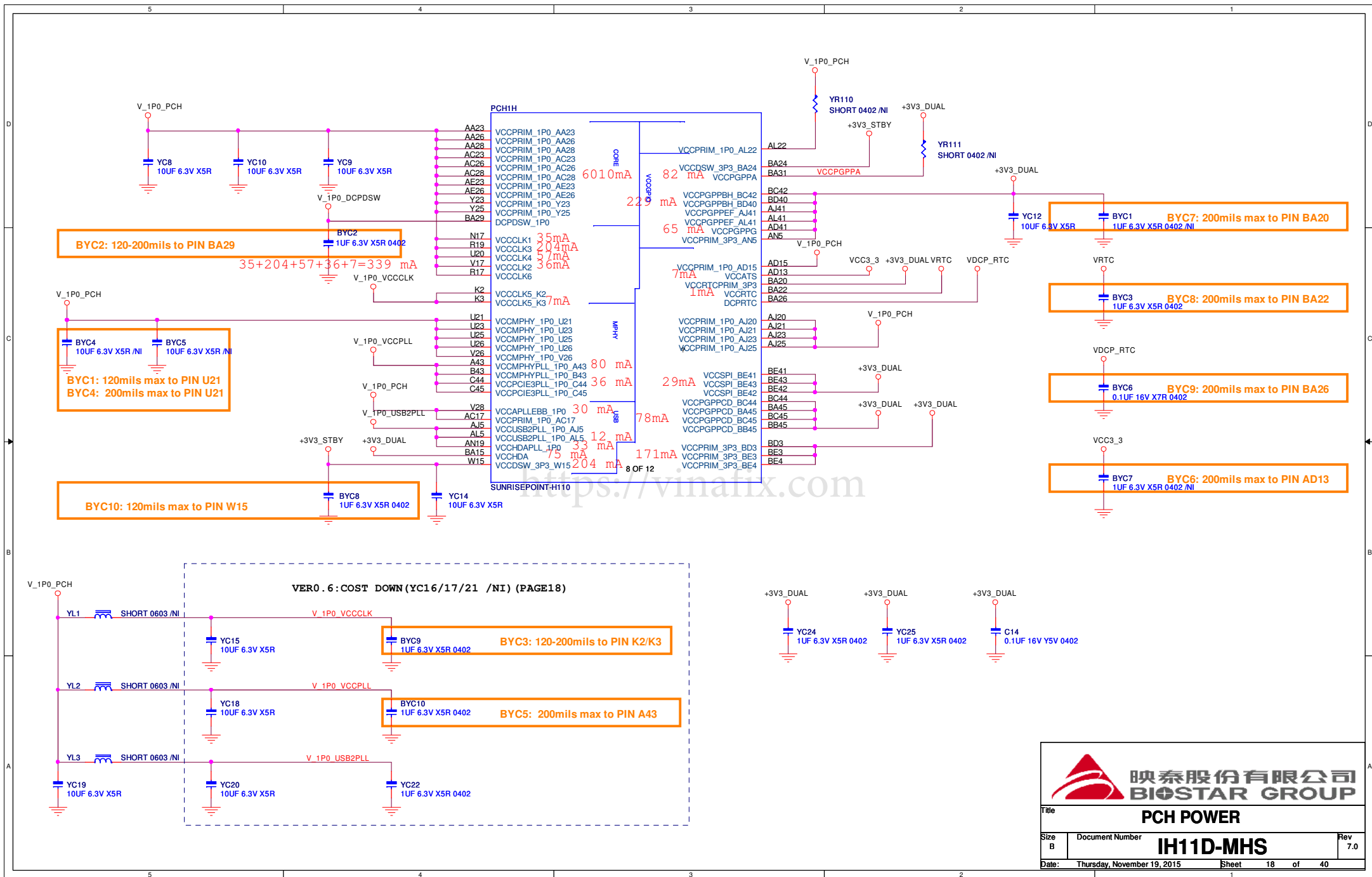


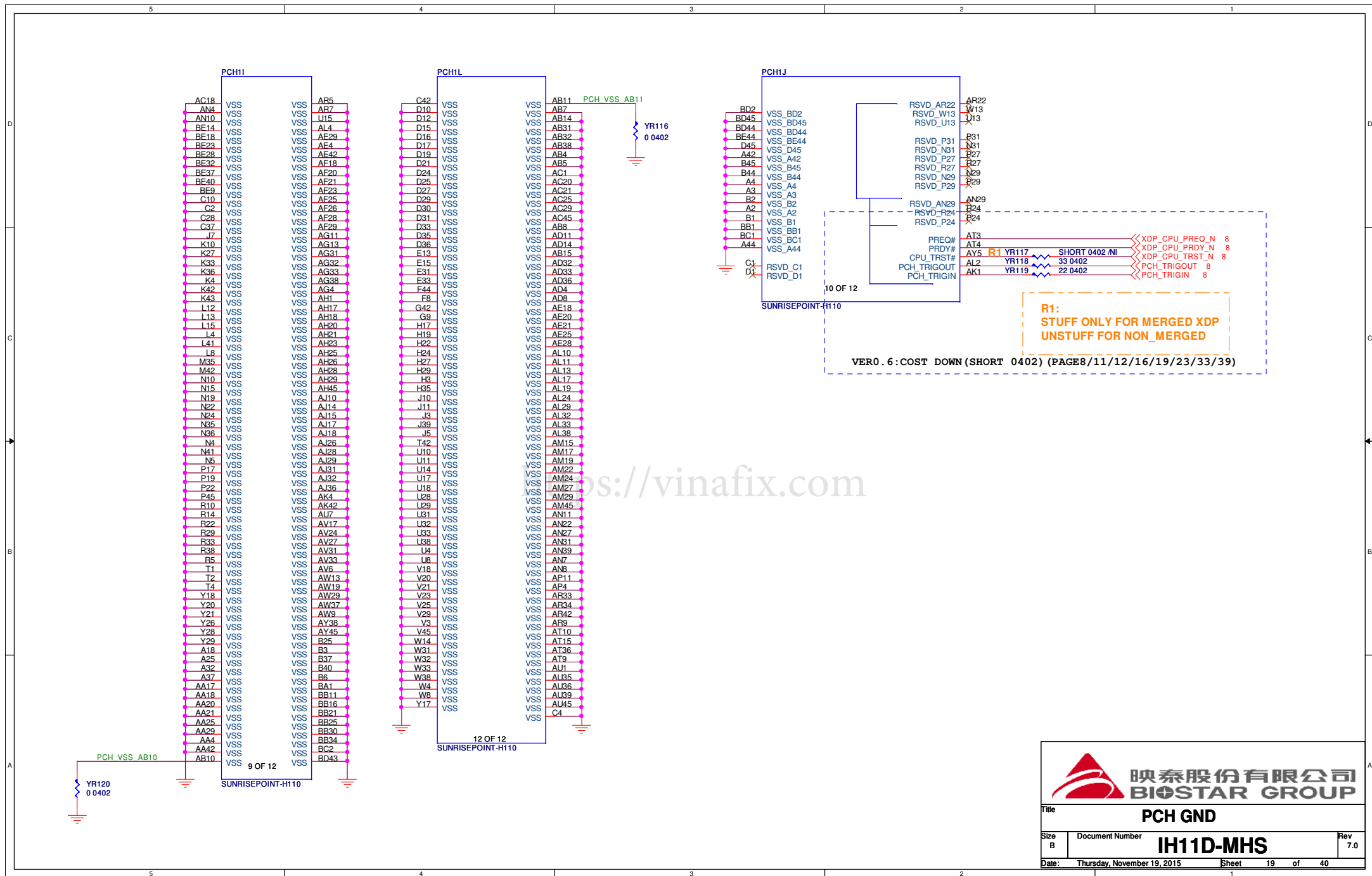


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Date: Wednesday, November 25, 2015	Sheet 16 of 40	





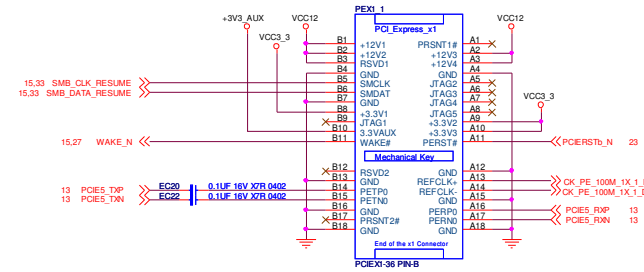
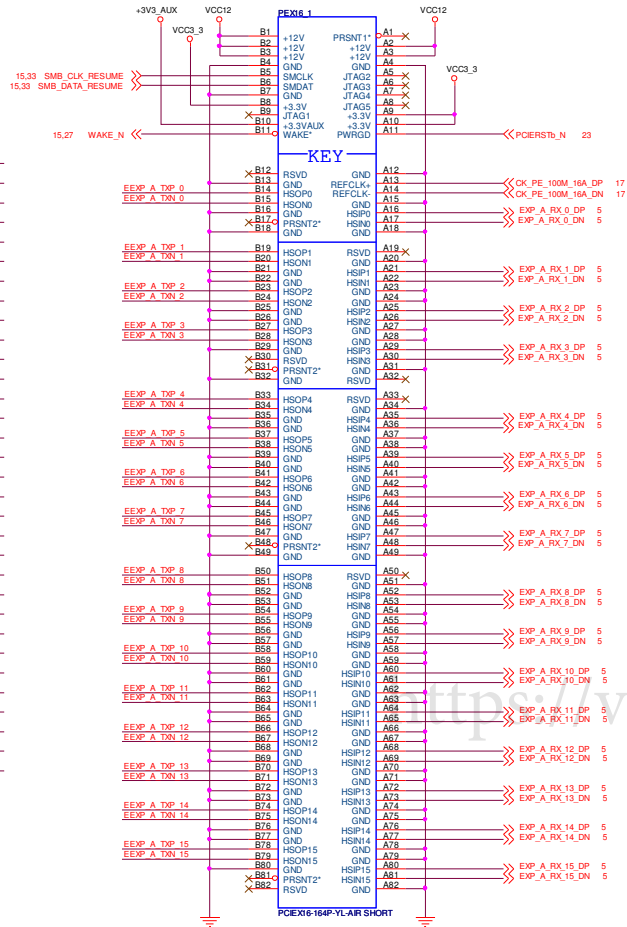




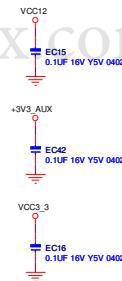
## SLOT PART: E+Reference

Value:180 nF - 265 nF

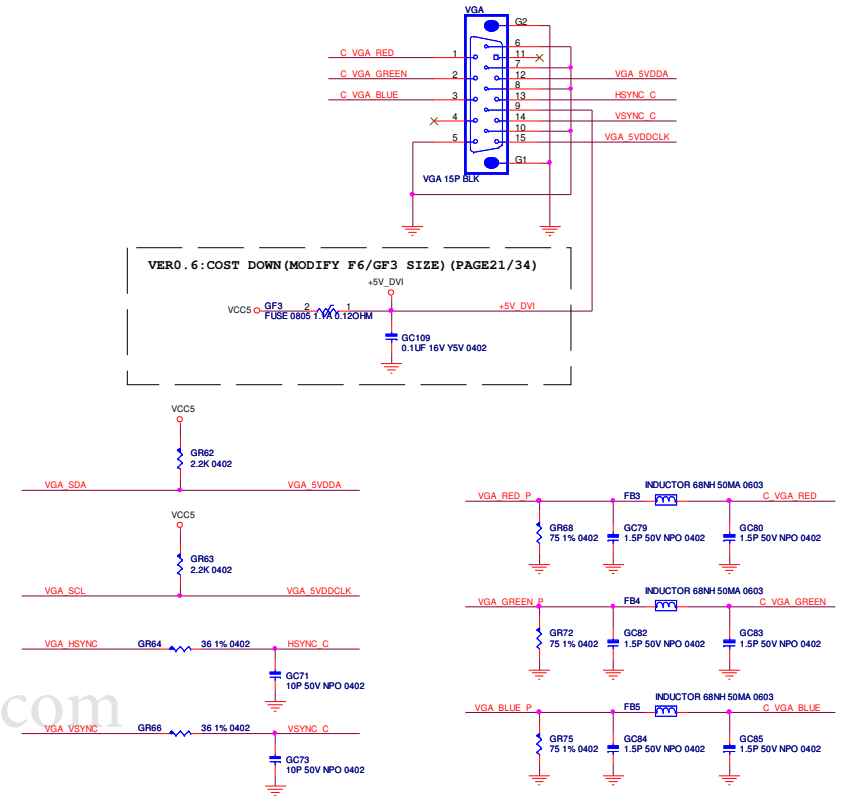
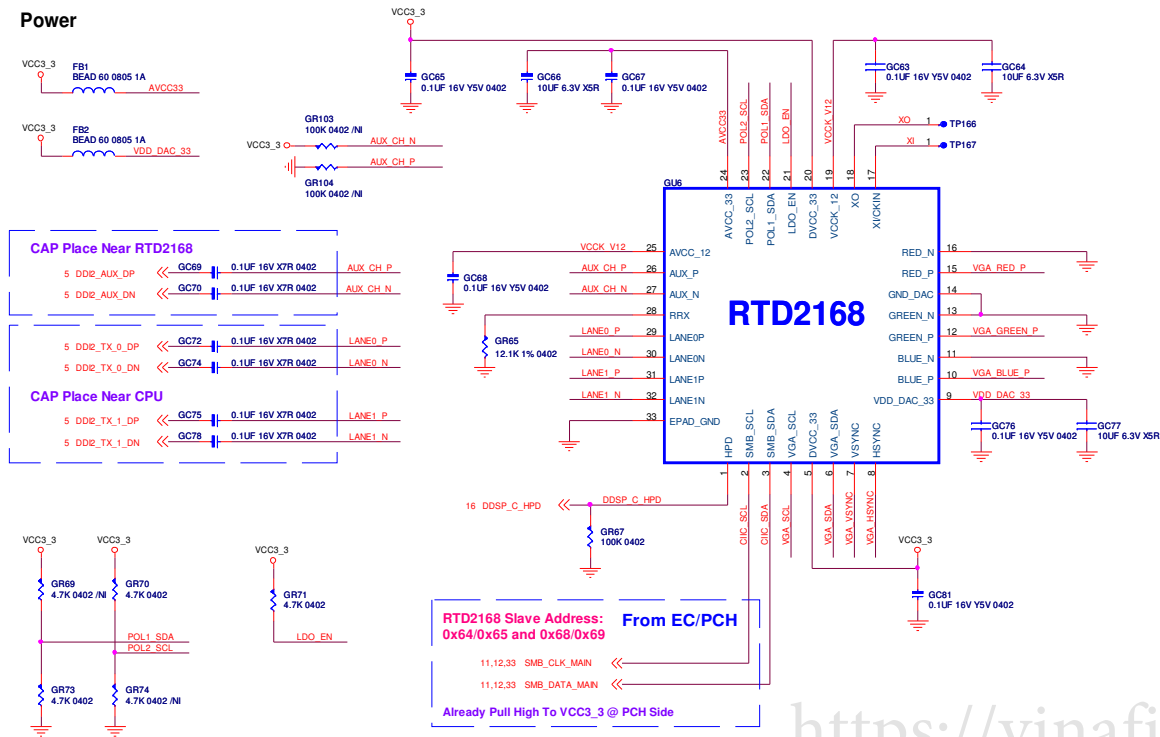
450 mils max to connector pin



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## Power



### Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	<b>EEPROM MODE</b>

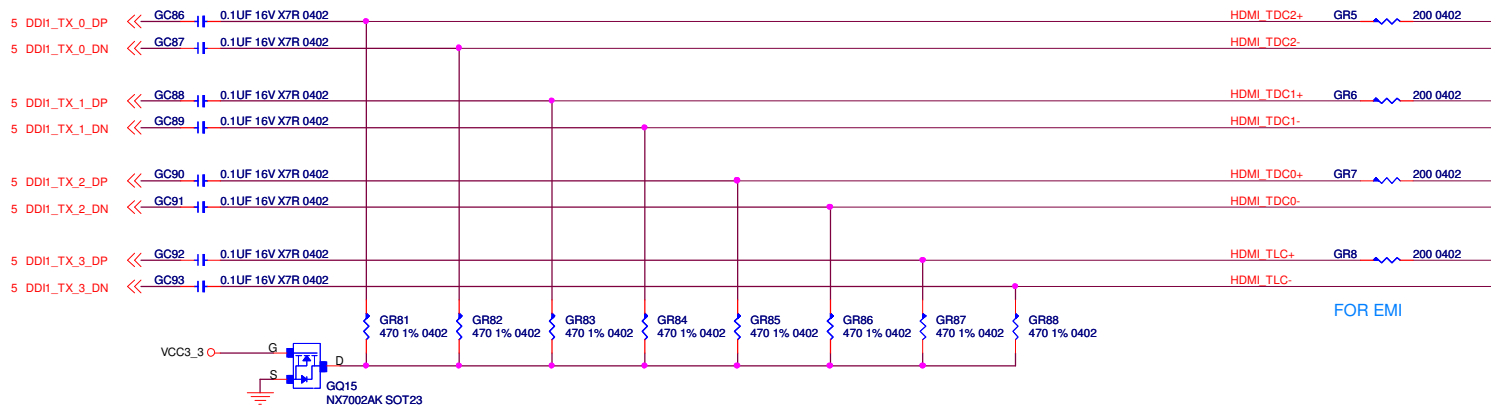
### Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	<b>VCCK_V12 from Embedded LDO</b>

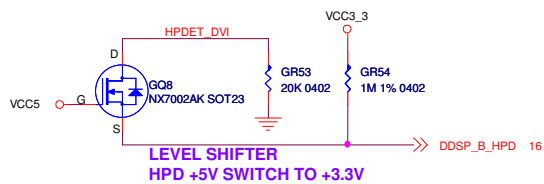
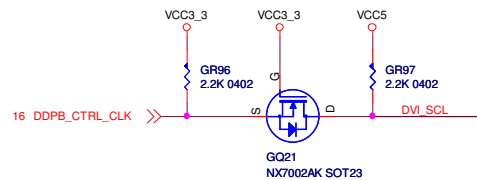
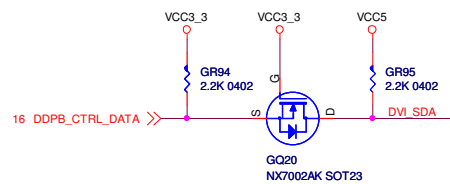
Table 12 Power consumption by using embedded LDO and embedded clock source

Active Resolution / Standby	DP Config.	Min	Typ	Max	Unit
1280x800x60(74.25-MHz)	1-Lane	-	400	450	mW
1600x900x60(103-MHz)	1-Lane	-	420	480	mW
1920x1080x60(148-MHz)	2-Lane	-	480	595	mW
Stand-by mode	-	-	7.5	8	mW

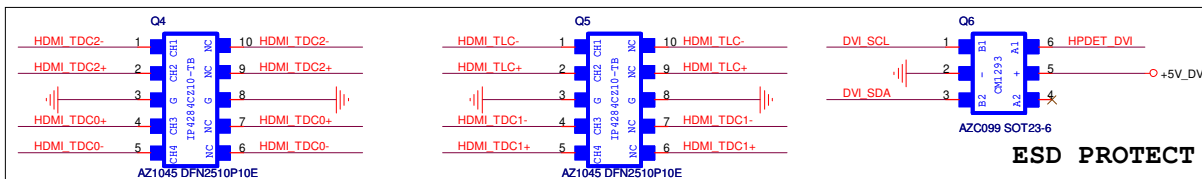
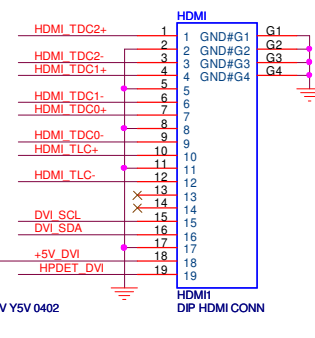




FOR EMI



# HDMI CONNECTOR

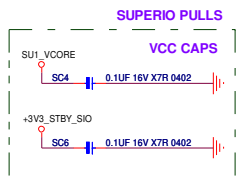
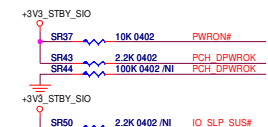
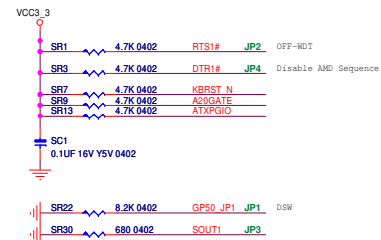


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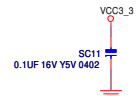
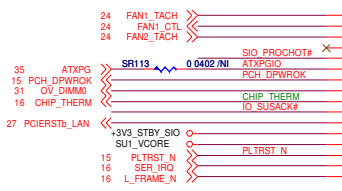
**HDMI**

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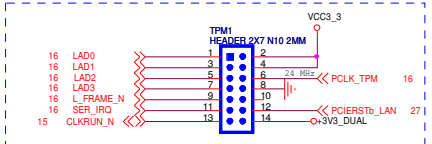
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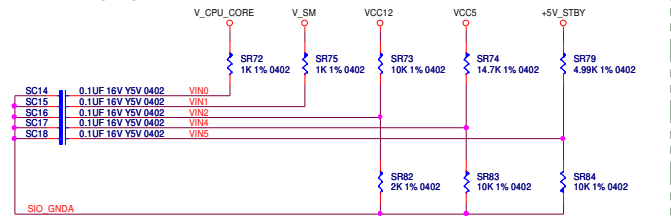
## IT8613E LQFP64



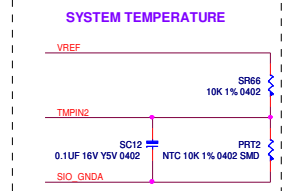
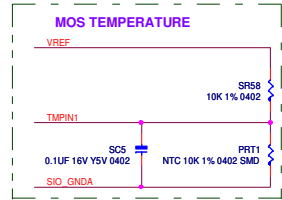
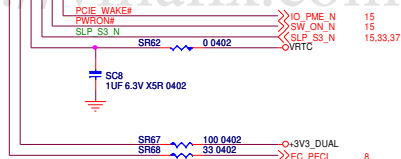
## TPM ASUS



## HARDWARE MONITOR



## 64-LQFP



## Power-On Strapping

Symbol	Value	Description
JP1	DSW_EUP_SEL	1
Pin-24		0
JP2	WDT_EN	1
Pin-56		0
JP3	FAN_CTL_SEL	1
Pin-58		0
JP4	K8PWR_EN	1
Pin-60		0

FAN\_CTRL2 not supported by JP3 FAN\_CTL\_SEL (EC index 6Bh default value always 80h)

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Title: SIO IT8613E

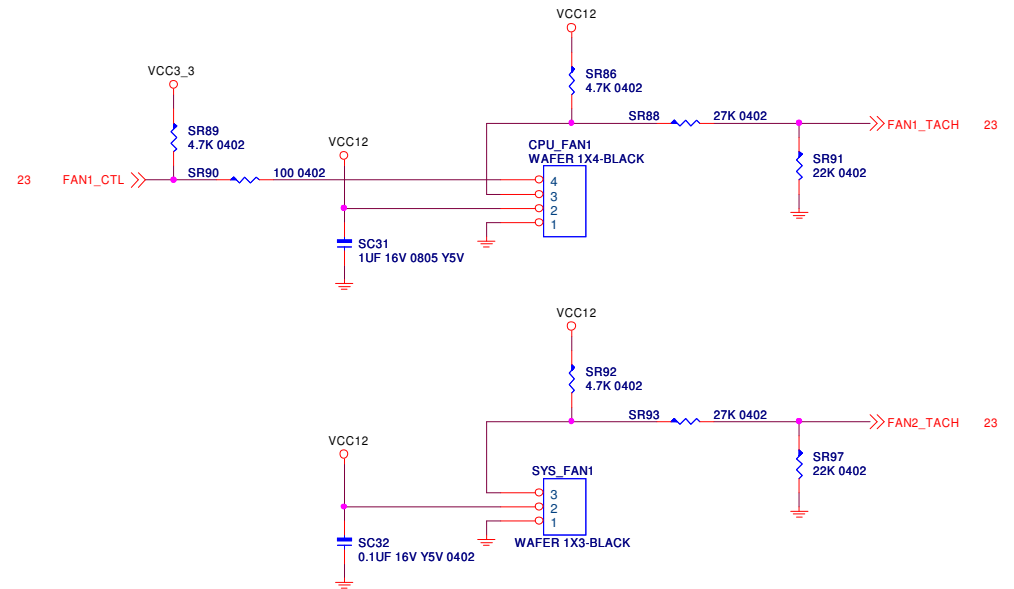
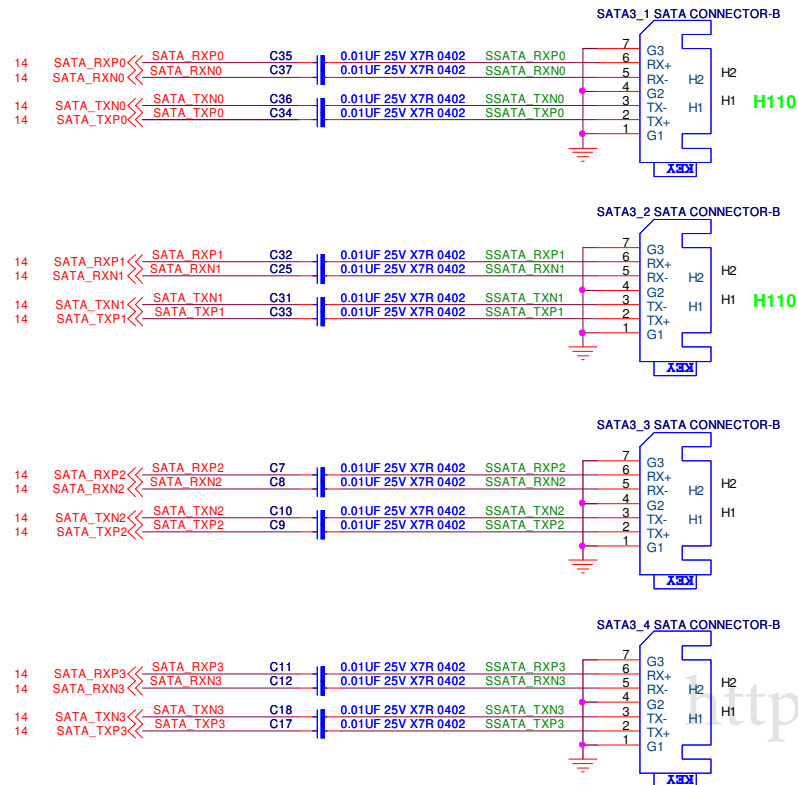
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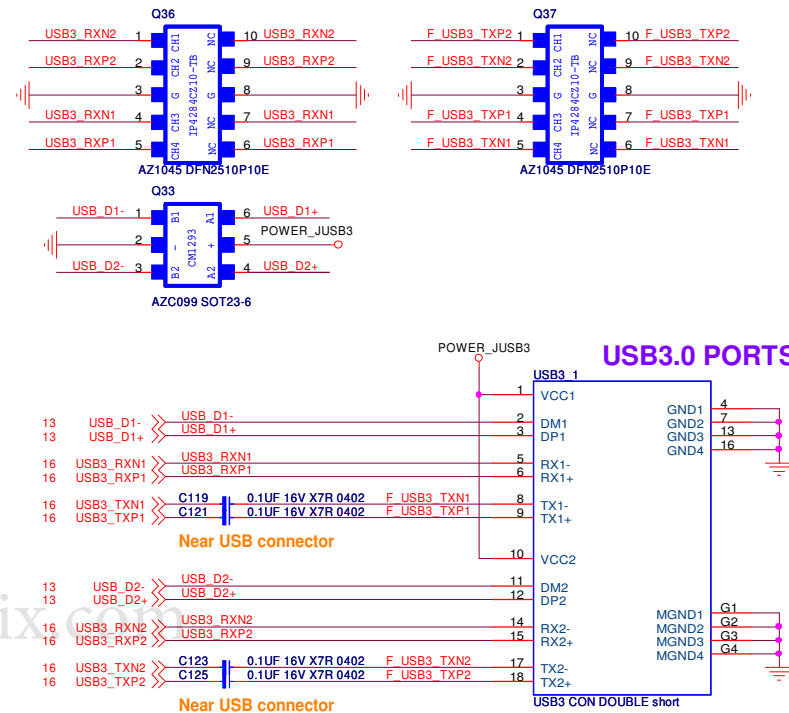
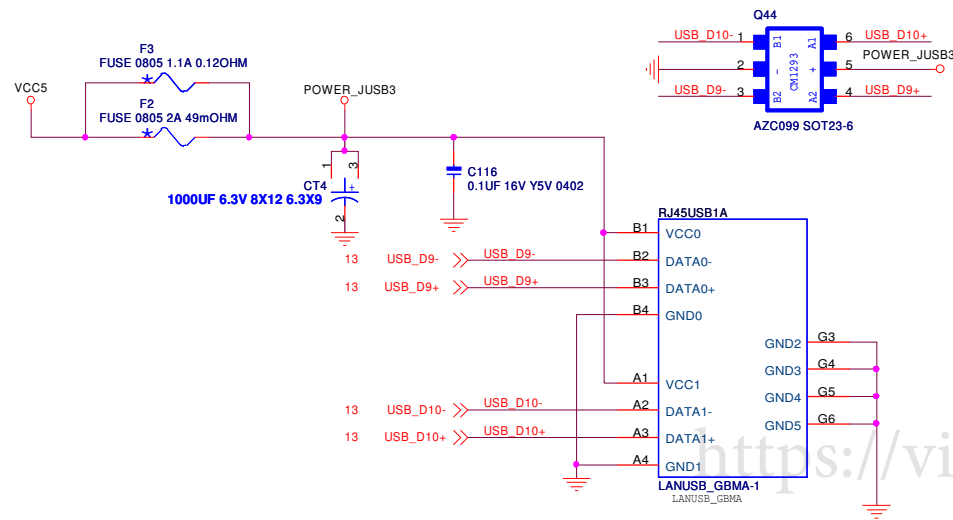
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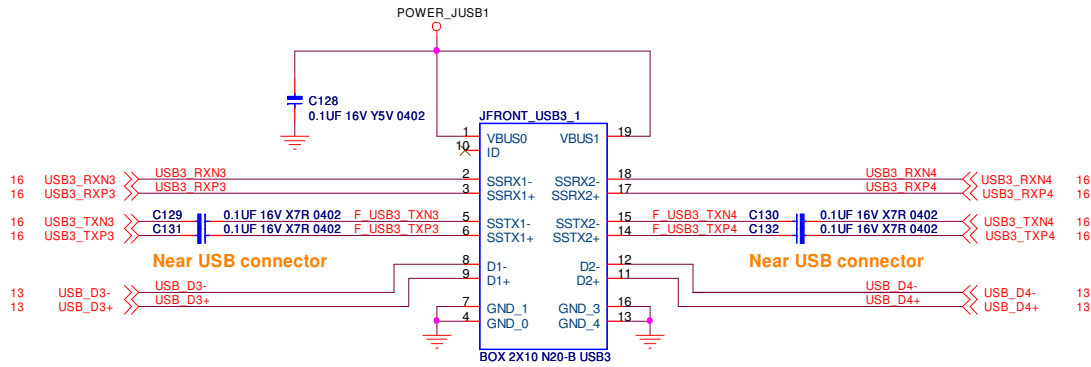
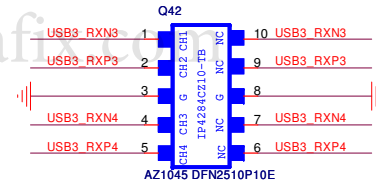
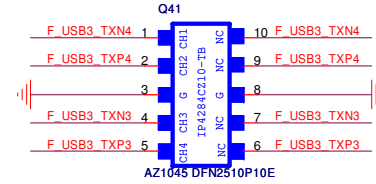
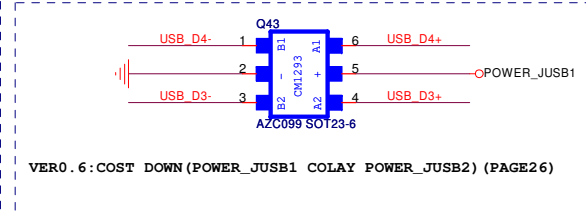
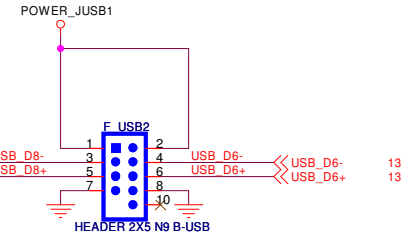
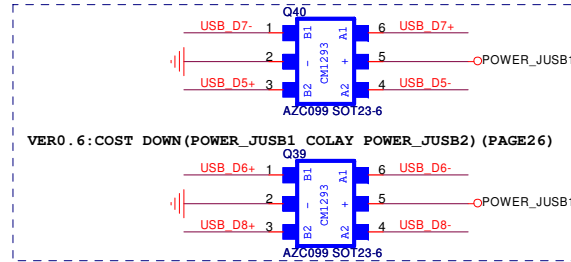
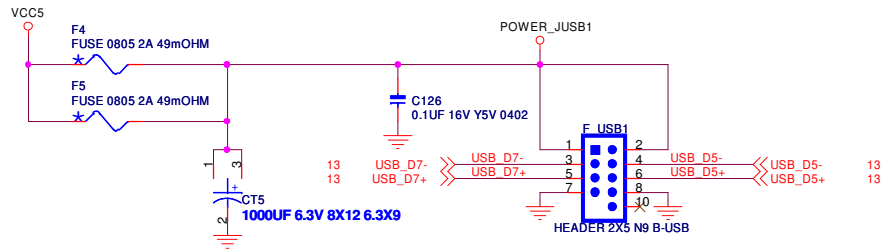


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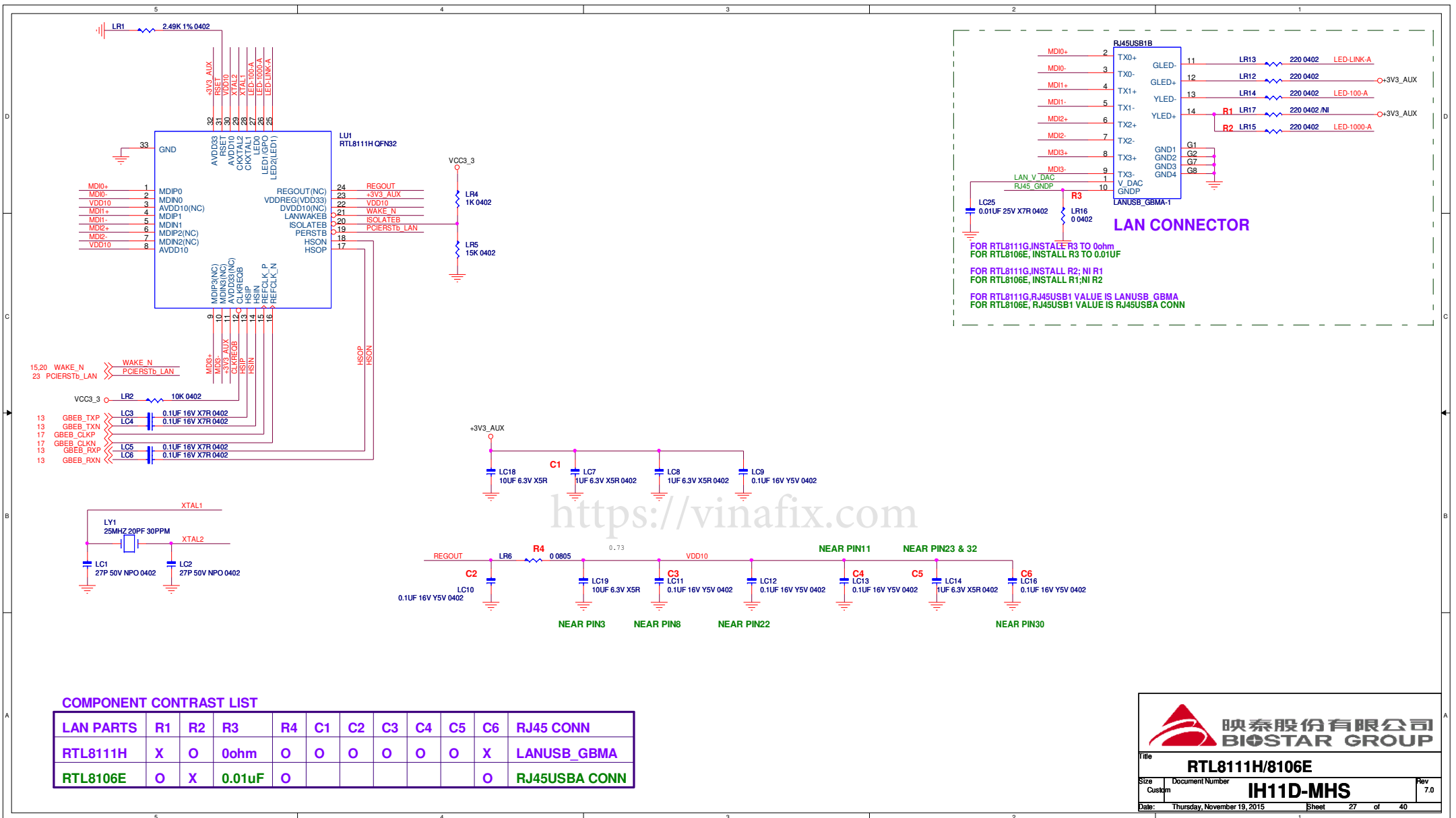


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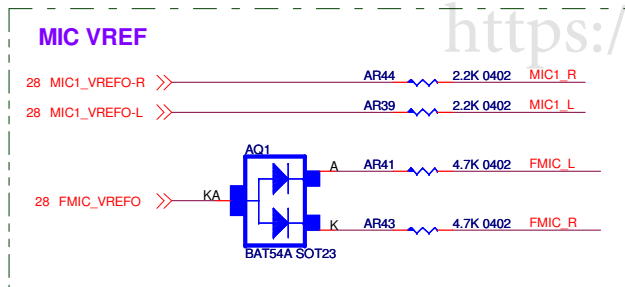
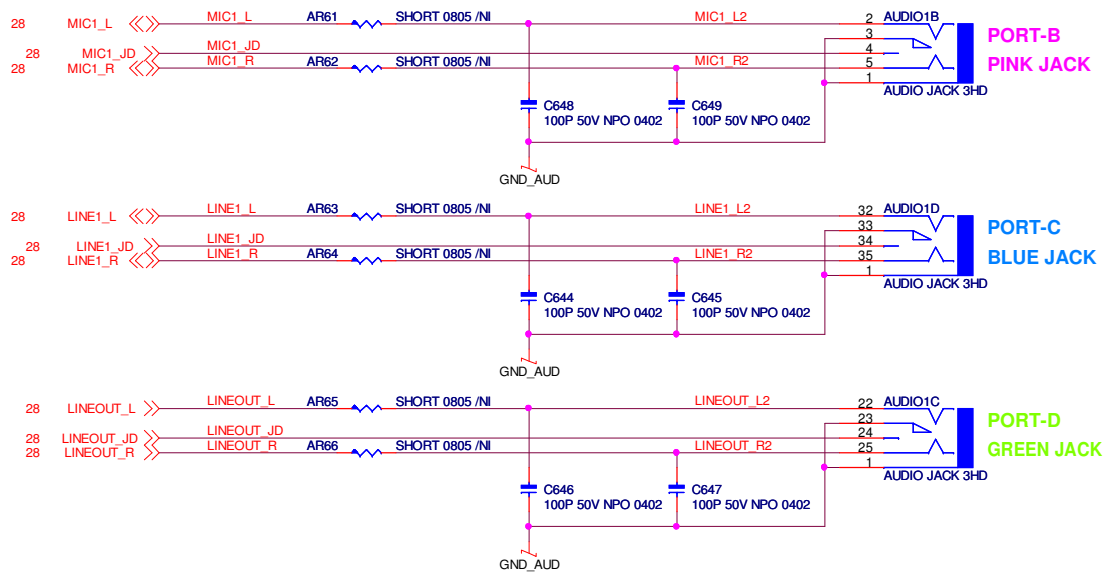
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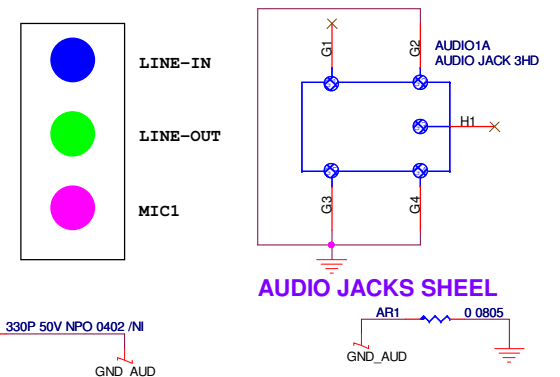
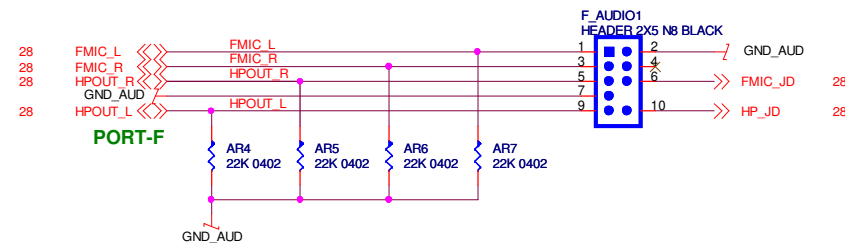
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Size B	Document Number <b>IH11D-MHS</b>	Rev 7.0
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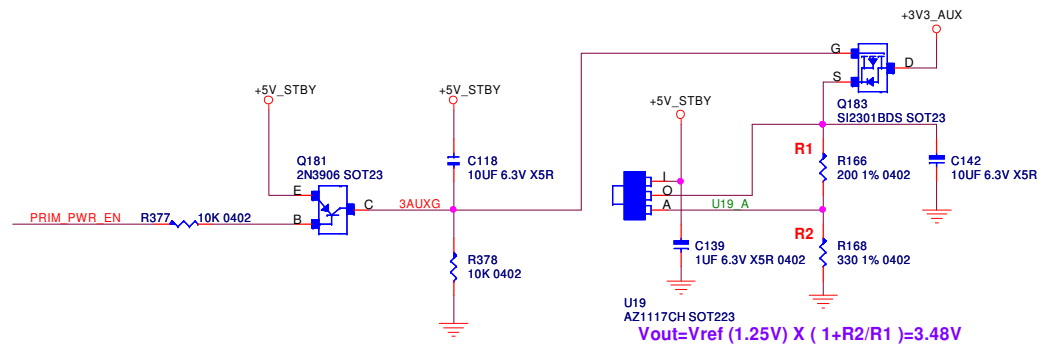
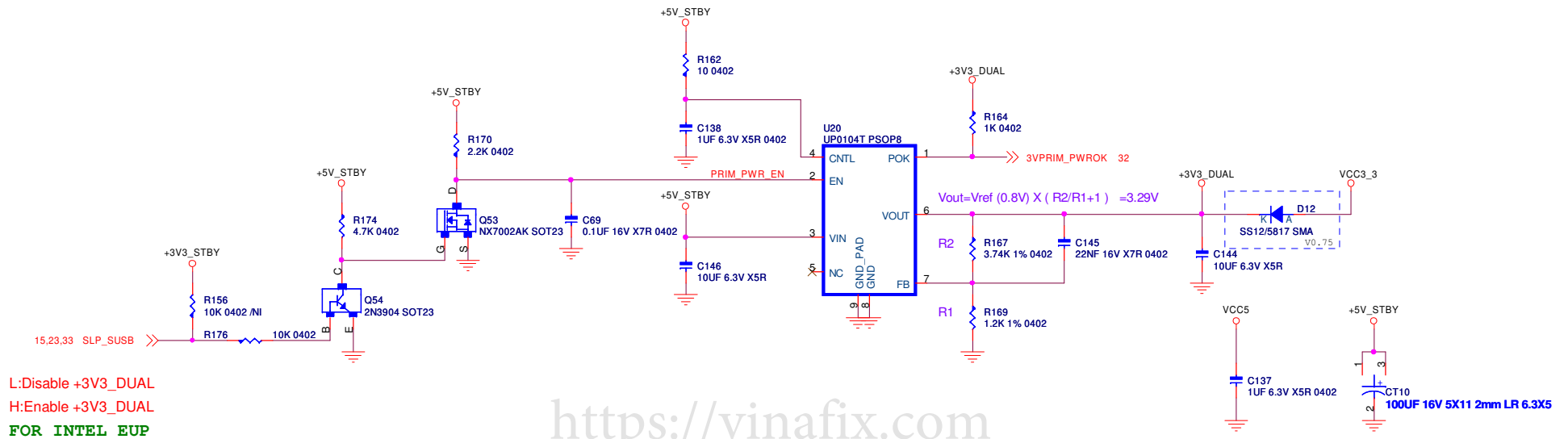
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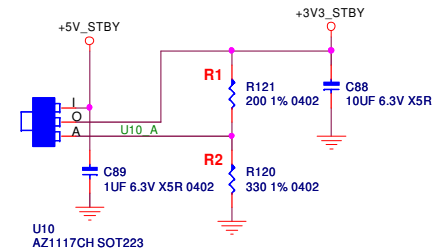
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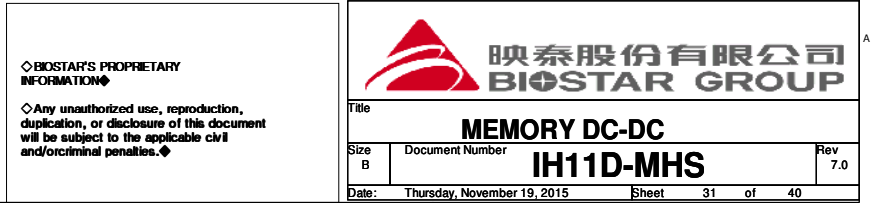
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Size	Document Number	IH11D-MHS	
Custom			
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		Rev	7.0



$V_{out} = V_{ref} (1.25V) \times (1 + R_2/R_1) = 3.3125V$

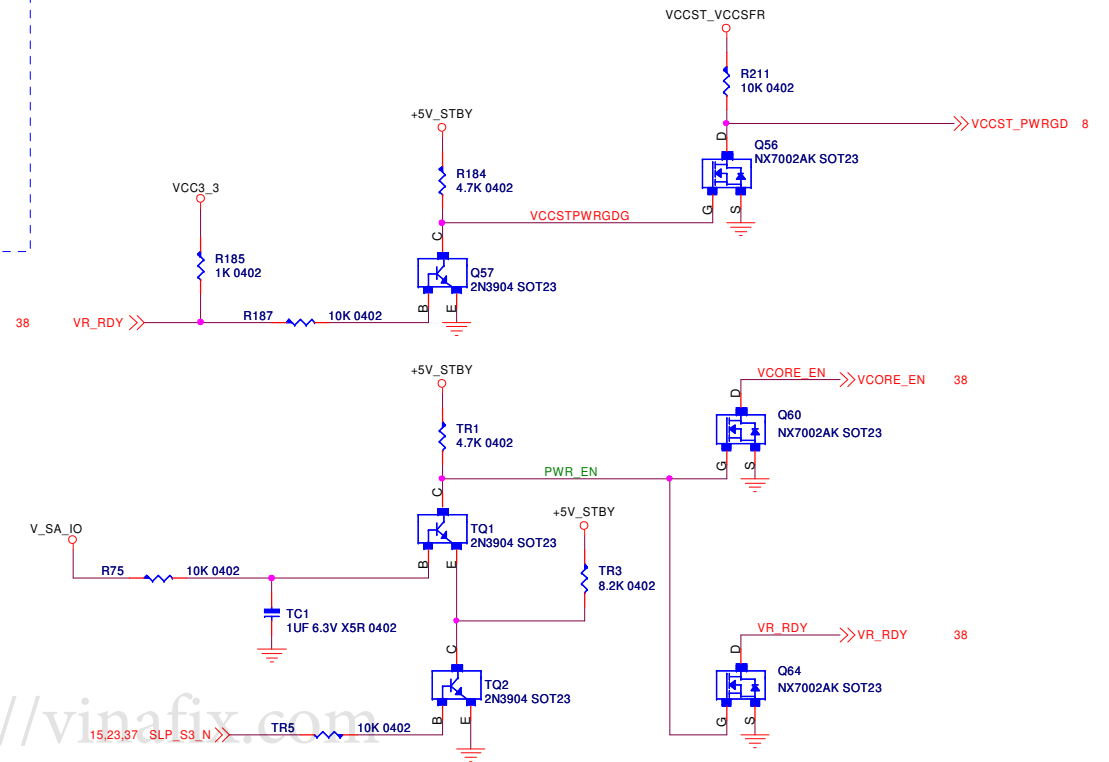
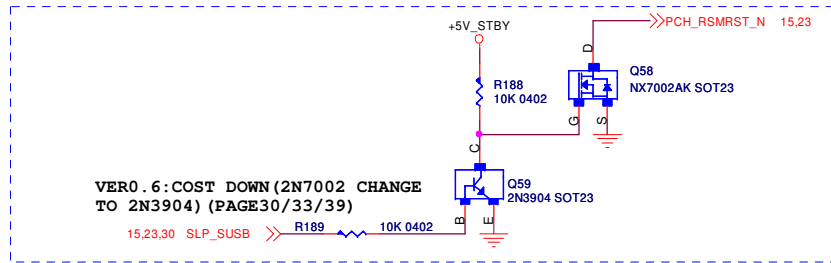


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15,23,37 SLP\_S3\_N >> TR5 10K

Q65  
NX7002AK SOT23

Q67  
NX7002AK SOT23

R192  
2.7K 0402

R193  
1K 0402

R194  
2.7K 0402

VCC3\_3

VCC12

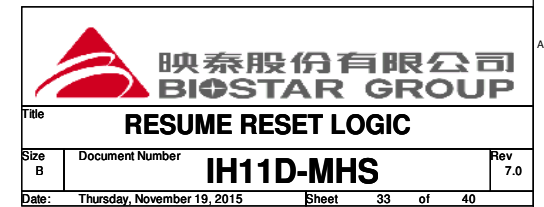
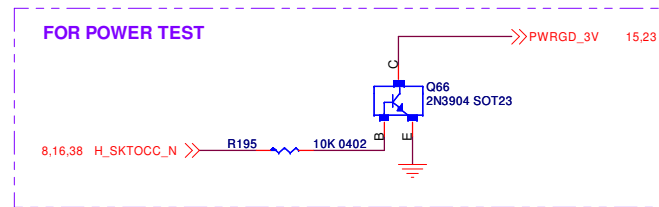
VCC3\_3

SMB\_CLK\_MAIN 11,12,21

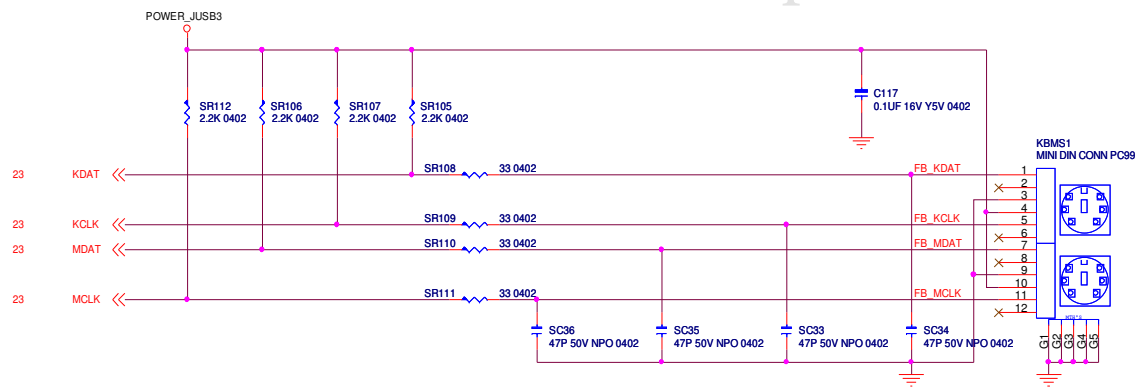
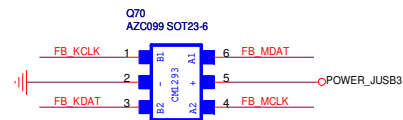
SMB\_DATA\_MAIN 11,12,21

15,20 SMB\_CLK\_RESUME

15,20 SMB\_DATA\_RESUME



## KEYBOARD & MOUSE



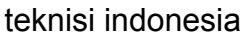
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## FP PART: F+Reference



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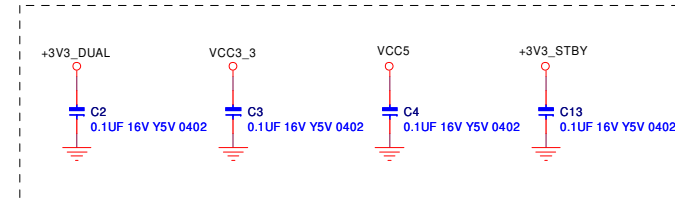
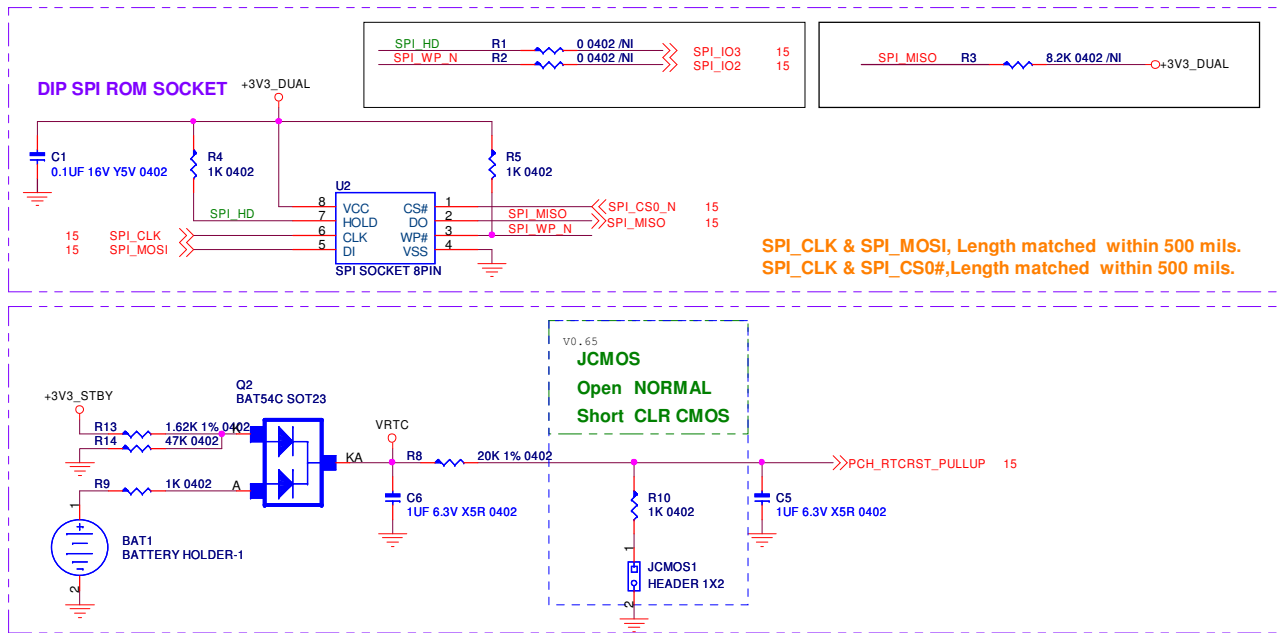
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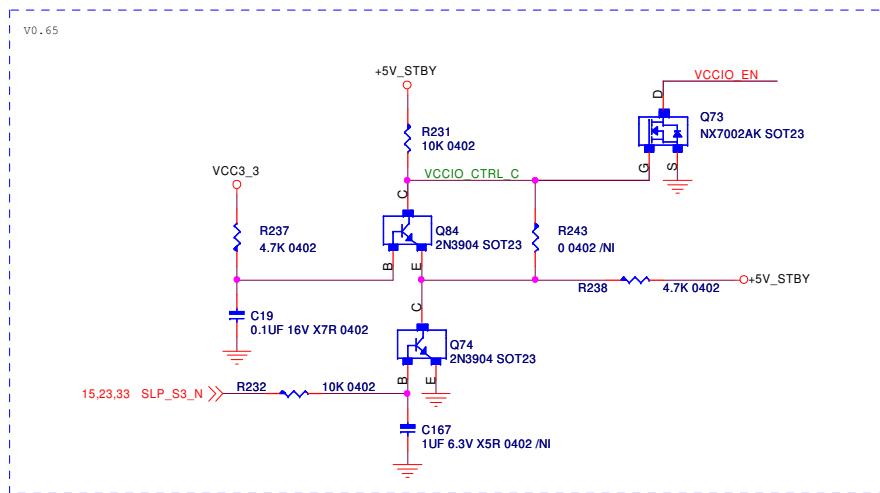
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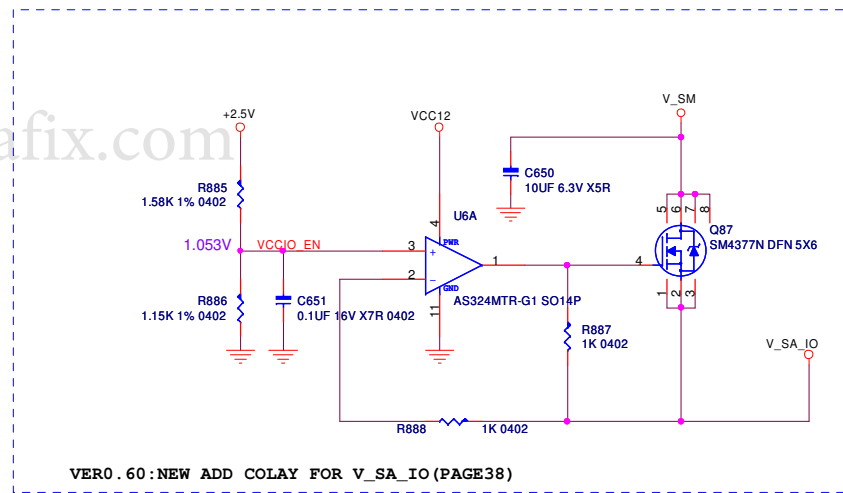


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<p>Title: <b>SPI ROM/RTC/BAT</b></p>		<p>Rev: <b>7.0</b></p>	
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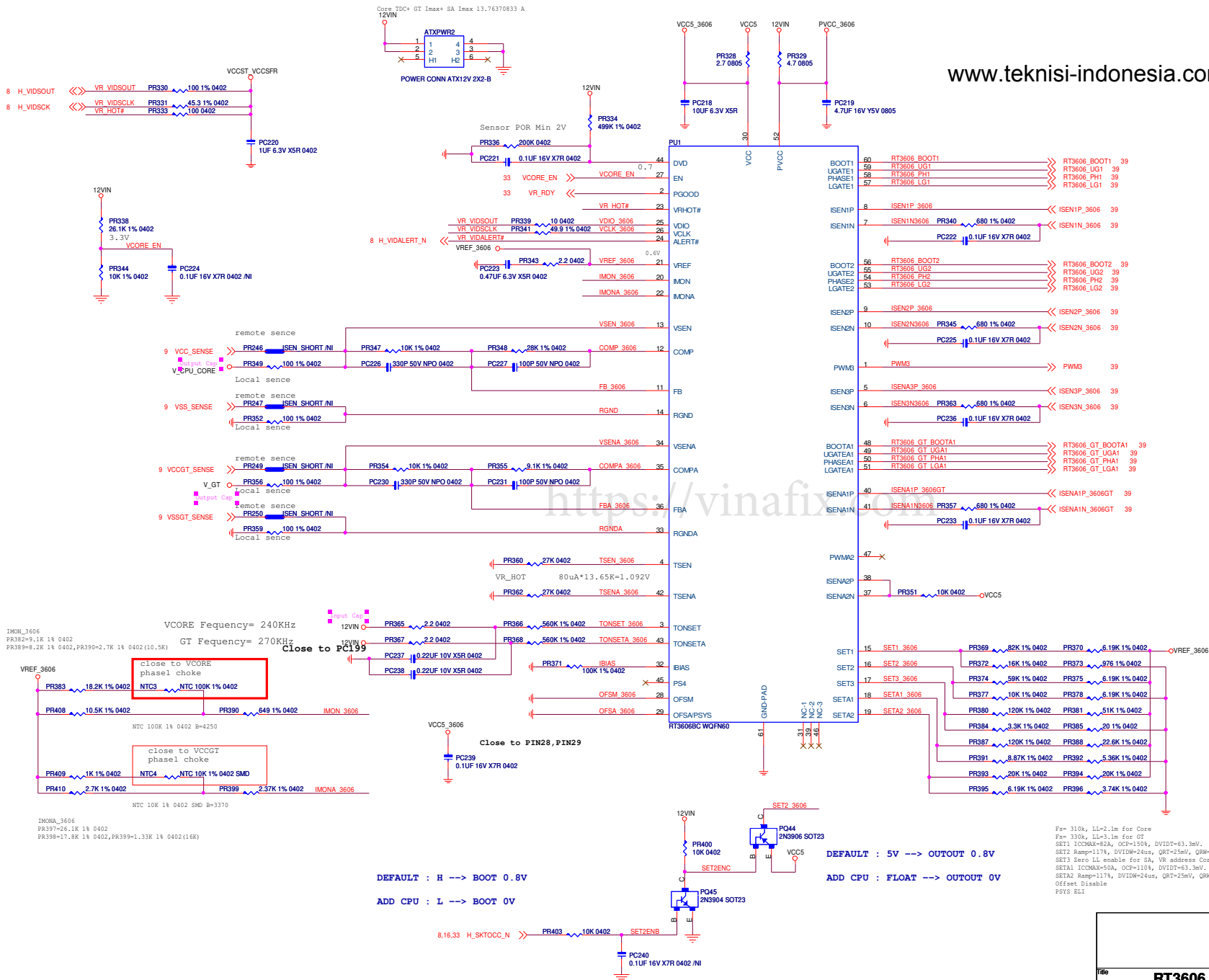
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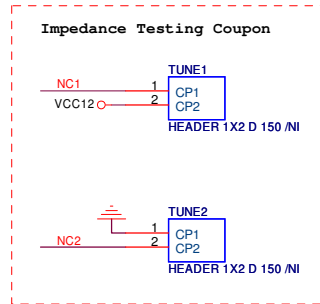
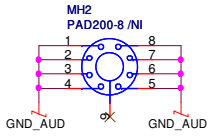
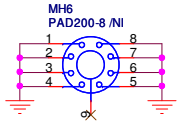
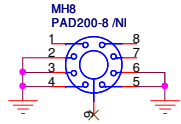
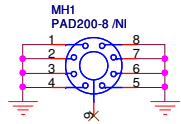
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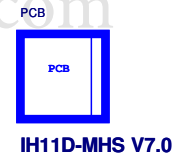
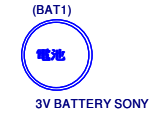
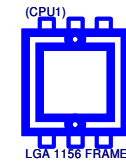
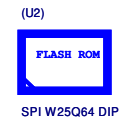


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